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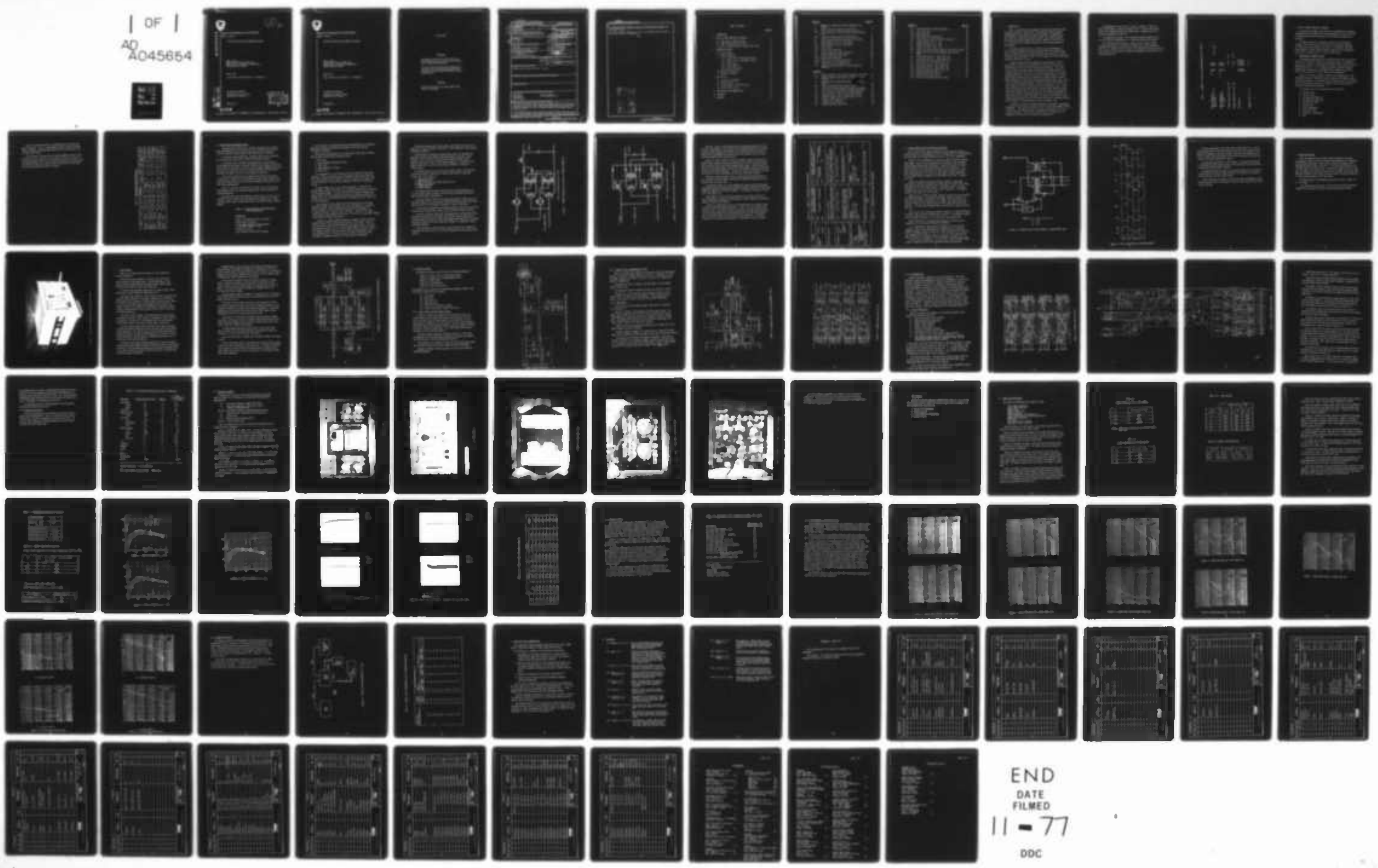

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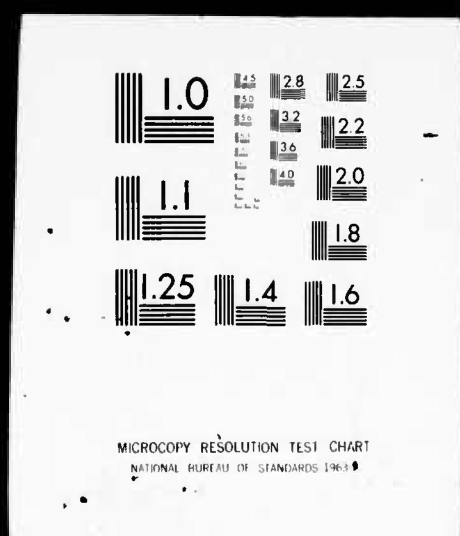

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Research and Development Technical Report

ECOM- 75-1324-F

TWO POINT FOUR KW DC/DC CONVERTER REGULATOR

John J. Biess
TRW Defense & Space Systems Group
Power Conversion Electronics Department
Redondo Beach, CA 90278

August 1977

Final Report for Period April 75 - December 76

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US ARMY ELECTRONICS COMMAND FORT MONMOUTH, NEW JERSEY 07703

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Dual Loop Feedback Control

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The 2.4KW DC-DC Converter/Regulator Power Module furnishes 0-75ADC over an output voltage range of 24 to 32 VDC from a nominal 20-40 VDC unregulated power source and can be used for battery charging from 5 to 75A. Remote output voltage sensing at the load circuit is provided to eliminate the IR drops of the power distribution cabling between the power module and the load.

A series inductor/parallel inverter power stage is used to provide the output power control and regulation input/output ground isolation and protection of the switching power transistors. The power supply is constructed in accordance with the Shelter-installed, Mobile →

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C-E Equipment destined for shelter or van use without the fans used for cooling. The internal electronics are modularized according to circuit function with provision for easy removal or repair.

Reliability, efficiency, weight and size achieved are approximately 8200 hours (MTBF), 84%, 73.3 lbs. 196 cu. ft., respectively.

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TABLE OF CONTENTS

1. INTRODUCTION

The U. S. Army Electronics Command is developing standardized power processing modules for application in the different power subsystem configurations being planned for digital equipment in communications, data handling, surveilance and weapon systems. This report presents the results of work performed under contract DAAB07-75-C-1324 for the U. S. Army Electronics Command to develop a DC-DC Converter/Regulator Power Module.

The specific objective of this contract was the development of a DC-DC Converter/Regulator that would provide precision; transient free 28V, 75A output power from a 20-40 unregulated input power bus; improve reliability and performance; reduce size and weight and reduce development, production and logistic costs.

A study of power processing techniques was performed in order to best satisfy the electrical, performance, reliability and mechanical characteristics for the 2.4kW DC-DC Converter Regulator. As a result of the review of the power stage configurations, available power semiconductors and power rating of an individual power module for the DC-DC Converter Regulator, a new transistor series inductor/parallel inverter power stage was developed that provided the necessary DC-DC conversion and the protection of the power semiconductors during steady state, transient and overload operating modes. The basic features of the DC-DC Converter stage is the power inductor which has two windings, one in series with the power source and the parallel inverter power transformer center tap and the second winding in parallel with the output filter capacitor. During the on-time of the power transistors, the difference between the input source and the power transformer is stored in the inductor primary winding and during the off-time of the power transistor, the energy stored in the inductor is transferred directly to the output filter.

A complete 2.4kW DC-DC Converter Regulator was designed, breadboarded and tested. The reliability analysis predicts a mean time between failures of 8200 hrs. The complete electrical design was packaged to fit into a 19 inch rack panel. The unit was fabricated into six electrical subassemblies and three auxiliary mechanical subassemblies.

The dimensions of the unit are 11 inches in height, 17 inches in width, 18.25 inches in length and weighs 73.3 lbs. The front panel dimensions are 19 inches wide and 12.25 inches high. A summary of the test results are presented in Table 1-I.

The demonstration model of the 2.4kW DC-DC Converter/Regulator fulfills the need for standardized U. S. Army Power Processing Equipment.

The following sections present a summary of the review of power processing techniques as applied to the 2.4kW DC-DC Converter/Regulator (Section 2), a discussion of the electrical and mechanical design (Section 3) and a review of the electrical, thermal, electromagnetic and acoustic test results (Section 4).

TABLE 1-I SUMMARY OF 2.4KW DC-DC CONVERTER/REGULATOR TEST RESULTS

OUTPUT REGULATION DUE TO LINE (20-40V & LOAD (0-75A)	eo = 24	11mV	
	28	17mV	
	32	18mV	(22 to 40V)
OUTPUT REGULATION DUE TO TEMPERATURE (0 - 120°F)	eo = 24	47mV	
	28	16mV	
	32	32mV	
CURRENT REGULATION AT 75A LIMIT		+2.1A, - 1.8A	
CURRENT REGULATION AT 25A LIMIT		+2.5A, - 4.5A	
EFFICIENCY AT	5A	74 MIN	
	25A	85.9 MIN	
	50A	86 MIN	
	75A	83 MIN	
STANDBY LOSSES (IO = 0)		13.7W	

2. STUDY OF POWER PROCESSING TECHNIQUES

A study was performed on the electrical, performance and packaging requirements for the 2.4kW DC-DC Converter/Regulator and the application of state-of-the-art power processing circuit designs and power semiconductors.

The design approach is influenced greatly by the input/output voltages, output power and the availability of high power components. The following section presents the results of the study of the power semiconductors, of power processing power stages and basic performance of the series inductor/parallel inverter power stages.

2.1 Semiconductor Component Study

The modulation power stage must by necessity operate at a high frequency (10 to 25kHz) to effect size and weight saving. The immediate concern is to identify a high-power semiconductor switch suitable for the intended application: It is therefore necessary to review the power semiconductor characteritics and determine the component limitations prior to the selection of a given power-stage configuration.

Due to the low input voltage of 20VDC, the saturated drop of the semiconductor must be minimized in order to obtain the highest possible conversion efficiency. The thyristor was eliminated early in the program, due to high saturated drop (2.0V), therefore, only a detailed view of the power transistor was performed.

The characteristics to be reviewed are the following:

- Voltage rating
- Current rating
- Maximum power capability
- Secondary breakdown area
- Rise and fall time
- Storage time
- Drive requirements
- Saturation drop
- Mechanical configuration
- Cost

Table 2-I presents the data on the commercially available high power transistors. Due to a developmental nature of these high power devices, addequate characterization does not exist and the unit costs are high at this time.

The conclusion of this study was that two 2N3066 transistors from RCA would be used in parallel for each power switch used in the DC-DC Converter/Regulator and as the high power semiconductor technology would be further improved, they could be easily incorporated in the present DC-DC Converter/Regulator electrical design.

TABLE 2-I POWER TRANSISTOR CANDIDATES CHARACTERISTICS

PART NO.	MFG. NO.	V_{CBO}	I_c MAX	SATURATION I_c	SATURATION V_{ce}	F_T	T_D Delay Time μs	T_R RISE TIME-μs	T_f FALL TIME μs	T_S STOR-AGE	COST 1-24	CORRESP. NO.
SDT 5843	Solitron	100V	200A	50A	0.6V	10MHz @ 5A	.07	.4	0.8	0.8	$157.50	TO114
2N5928	Power Tech	120V	100A	100A	1.0V	1MHz		2.5	2.5	3.0	219.00	TO114
PT9503	Power Tech	120V	200A	200A	.35V	1MHz		3.0	3.0	3.0	328.00	Special Case
SCA 100-120	Semicoa	100V	100A	30A	.5V	30MHz	.350	.25	.2	.4	64.60	TO-3
2N 3066	RCA	120V	40A	40A	1.0	50MHz		1.0	.5	1.5	39.00	TO-3

2.2 Power Stage Configuration Study

The power stage configuration is greatly influenced by the type of power semiconductors used to provide the on-off switching necessary for dc to ac inversion and input-output power modulation and regulation.

In transistor power technology, the power switch can be controlled by the application and removal of power from the base terminal.

In thyristor power technology, the power switch can be turned on by the application of power to the gate terminal but the power switch turn-off can only be performed by external circuitry and/or components that force the thyristor current to zero for a minimum time period after which the thyristor can remain in an off or non-conducting condition.

Due to the elimination of the power thyristor due to its high saturated drop in comparison with the minimum dc input supply voltage; only transistor power processing circuits were reviewed for application to the DC-DC Converter Regulator.

Table 2-II shows the classification of power stages for transistor semiconductors that were reviewed for application in the 2.4KW DC to DC Converter/Regulator.

Paralleling and phase displacement of power stages will also be considered in order to reduce the input/output filter weight and to reduce the peak current and/or voltage stressing of the respective power semiconductors.

TABLE 2-II CLASSIFICATION OF TRANSISTOR POWER STAGE CONFIGURATIONS

Transistors

Center Tap Transformer Parallel Inverter

Bridge Parallel Inverter

Series Chopper Regulator with Centertap Transformer Parallel Inverter

Buck-Boost Converter

Series Resonant Inverter (Half Bridge)

The selection of an optimum power stage configuration for a particular application initially involves the elimination of the vast majority of potential candidates.

The specified requirements for this application, which most influence the selection of power stage configuration are:

- Efficiency
- Input & Output Voltage Requirements
- Power Level
- Power Component Limitation
- Reliability

The requirement for "free convection" cooling makes high efficiency important. Power dissipation within the package significantly impacts on unit size and weight since finned heat sinks are required to transfer heat to the surrounding air and maintain components within their temperature ratings.

In power systems such as this, where prime power is derived from battery energy storage, the quality of the system is measured by utilization of the energy available. The cost and bulk of the energy storage system usually offer sufficient leverage on efficiency to warrant increased complexity and cost in the converter process to accomplish overall system cost and size reductions.

The high power rating combined with the requirement for continuous operation at 20Vdc input voltage places severe requirements on switching devices, magnetics, and distribution cables within the packaged unit. DC input current will range as high as 140 Amps. Currents of this magnitude require large conductors which make it difficult to route power through input breakers and about the package.

The use of a single switching element as opposed to several carrying proportionally smaller currents results in high, "skin effect" losses in wires carrying AC currents and complicates the thermal design. The high concentration of power loss in a single element makes it difficult to maintain thermal gradients from the active area of the semiconductor switch to the outside world. The use of several switches or modules divides the power loss between elements and allows physical displacement.

Breaking the power stage up into several lower power level units also reduces wire sizes, minimizes "skin effect" losses, mechanical wiring routing and terminal problems.

High frequency transformers carrying high currents are mechanically difficult to build and in general have poor magnetics coupling. Large conductor size is difficult to bend and form around the small radius peculiar to the small size of high frequency magnetics. In addition, the power concentration in the part poses special problems of "Hot-Spot" thermal control.

An important measure of the quality of a power stage is the amplitude of currents switched. Selection of a power stage with the lowest RMS current levels will result in:

- Lower part stresses
- Smaller EMI and
- Lower I^2R losses in a given conductor size
- Reduced audio noise
- Higher efficiency
- Lighter weight

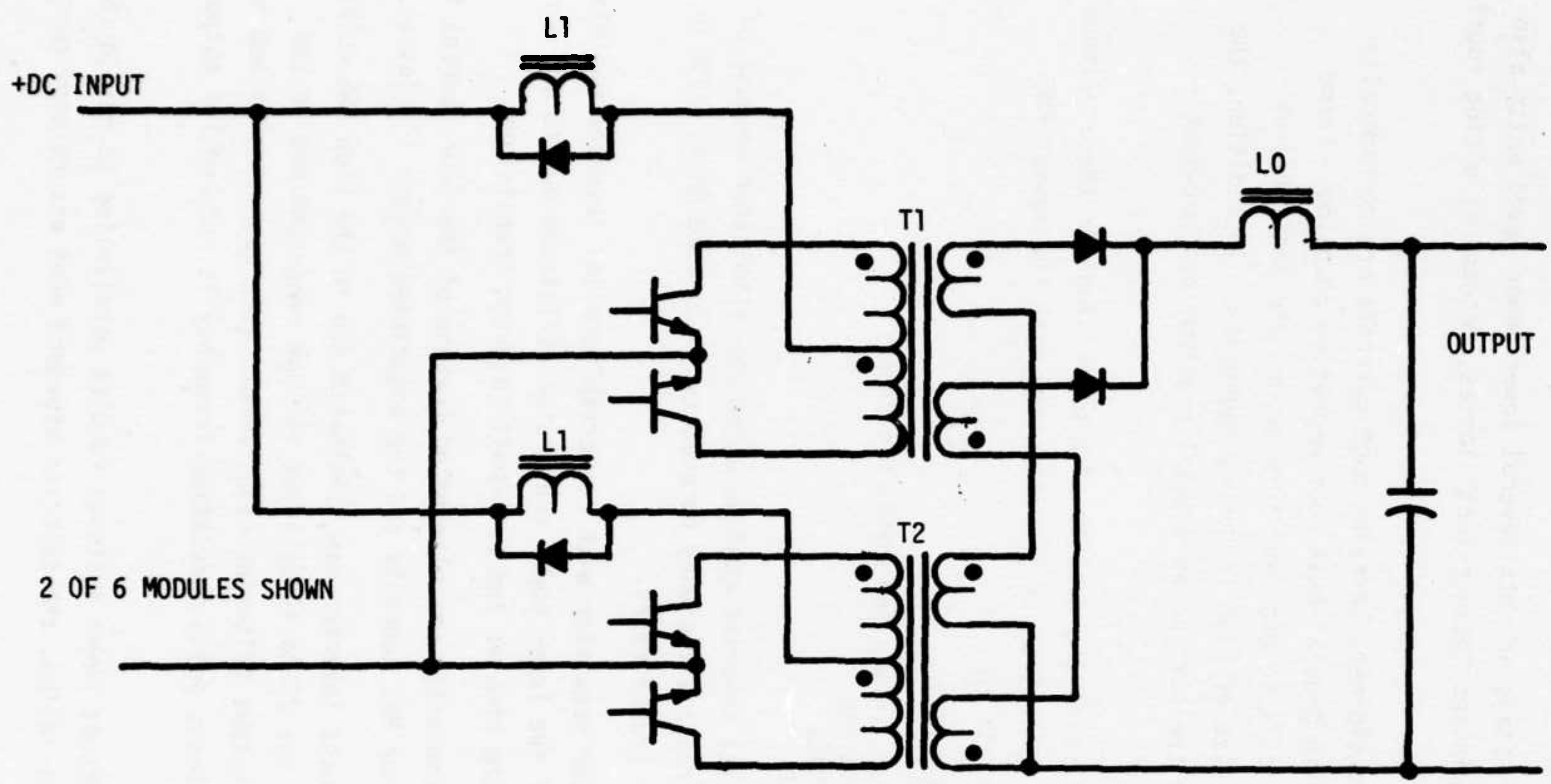
The bridge parallel inverter configuration was eliminated because of its lower power conversion efficiency because two saturated drops were in series with the power transformers.

The series chopper regulator with centertap parallel inverter was also eliminated because of the lcwer power conversion efficiency due to the series power transistor in the chopper and push-pull inverter transistors.

The Buck Boost Converter was eliminated because of the poor current form factor and their higher RMS currents and the associated higher I^2R losses.

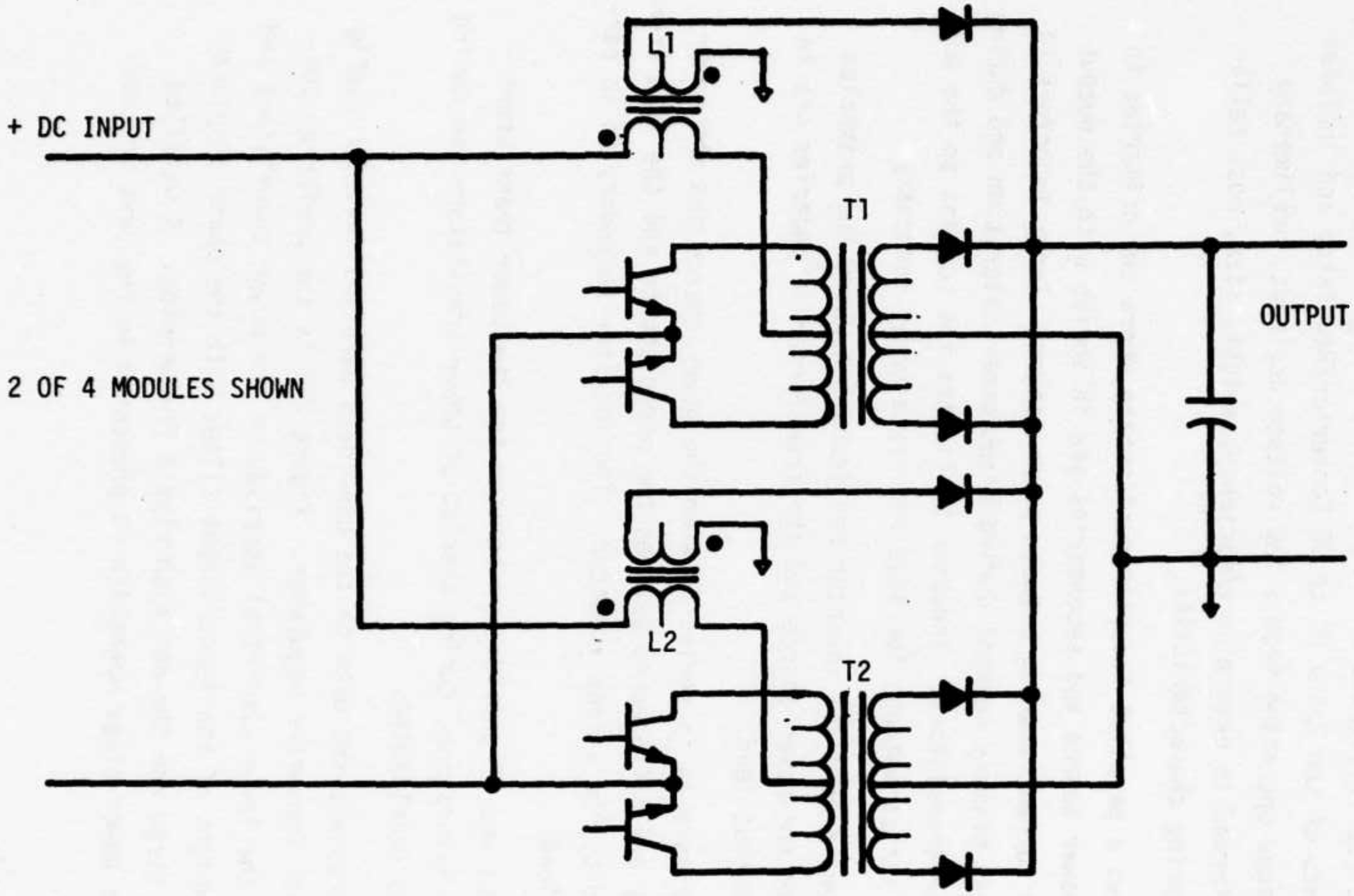
The series resonant inverter was sliminated due to the high RMS current that would flow over the 20 to 40Vdc input voltage range and due to the increased input and output filtering requirements when operating at low output power level and the basic pulse modulation frequency is reduced for output regulation purposes.

Since transistors as power switches require paralleling to obtain the required high current rating, the selected approach must assure good current sharing.



NOTE: All Modules Driven in Phase

FIGURE 2-1. MODULAR CONVERTER WITH SERIES AC SECONDARY CONNECTION



NOTE: Modules are phase displaced

FIGURE 2-2. MODULAR CONVERTER WITH PARALLEL DC SECONDARY CONNECTION

Figures 2.1 and 2.2 illustrate the basic configuration that can fulfill the basic requirements of the 2.4KW DC to DC Converter/Regulator and includes transistor power stages operating from a low voltage dc input, preliminary designs will be performed to determine efficiency, weight, size, cost reliability and manufacturing characteristics.

Figure 2-1 shows a parallel inverter configurate where the primaries in parallel with the power source and secondaries are in series with the output load to ensure load current sharing between power stages. Input inductors L1 and L2 limit the peak primary current during transformer saturation and during overlap of the power transistors. Inductor LO filters the current to the output load and is in series between the load and transformer secondary.

Figure 2-2 shows a parallel inverter configuration where the primaries are in parallel with the power source and the transformer secondaries are in parallel with the output load.

An inductor primary is in series between the power source and the power transformer primary and differences between the power source and the load transformer are absorbed by the series inductor. The inductor secondary is in parallel with output load.

The inductor L1 and L2 provides protection for the power transistors during transformer saturation, during overlap of power transistors and during output starting and overloading.

Table 2-III presents the data on the candidate parallel inverter configuration of the DC-DC Converter Regulator. Figure 2-2 is the preferred configuration due to the lower electrical stresses on the power transistors and due to the lower weight of the input/output filter with the phase displacement of the power stage and the net high ripple frequencies. A detailed discussion of this power stage operation is presented in the next section.

TABLE 2-III. TRADEOFF OF POWER AMPLIFIER CONFIGURATION

TRADEOFF	FIG.2-1 - SERIES CONNECTED AC SECONDARY (Secondary series inductor)	FIG 2-2 - PARALLEL CONNECTED DC SECONDARIES (Primary series inductor)
Transistor Stress: Current	24.7A Six modules. 12 Transistors	33.37A Four Modules 8 Transistors 16.7A Four Modules 16 Transistors
Transistor Stress: Voltage	80V	60V 60V
Load Current Sharing	Inherent in the circuit. Transistor & Transformer primary current limited by inductor & flyback rectifier.	Electronically forced load balance. Transistor & Transformer primary currents limited by input inductor configuration.
Transformer: Voltage	80V Across Push-Pull Primary	40V Across Push-Pull Primary
Transformer: Size	1	.6
Transformer: Circulating Current	Continuous current flow in all transformer windings. With circulating current returned to the power source.	Duty cycle controlled current flow with all currents delivered to the load.
Ripple Currents to Filter	<u>6 Modules</u> — <u>Filter Size</u>	<u>4 Modules</u> — <u>Filter Size</u>
• Input	49 Amp peak to peak — 1	33 Amps peak to peak — .3
• Output	25 Amp peak to peak — 1	1 Amp peak to peak — .3
• Frequency of Ripple @ 10 kHz Module Frequency	20kHz	80kHz
Control Concept.	Constant Frequency (requires external ramp)	Variable frequency (no ramp required)

TABLE 2-III. CHARACTERISTICS OF POWER STAGE CANDIDATES

2.3 Series Inductor/Parallel Inverter Power Stage

Due to the new power stage configuration of the parallel inverter, a brief dicussion will be presented in order to understand the circuit operation and the current and voltage waveforms on each of the circuit components.

Figure 2-3 is the schematic for the series inductor parallel inverter power stage. The circuit includes the series inductor L with a primary and secondary winding, power transformer T, power transistors Q1 and Q2, output rectifiers CR1, CR2 and CR3 and output filter capacitor C. The power transistor are controlled by a driver stage to provide the correct pulse width modulation to satisfy the input/output voltage requirments. In this example both the inductor and transformer turns ratio is assumed to be one.

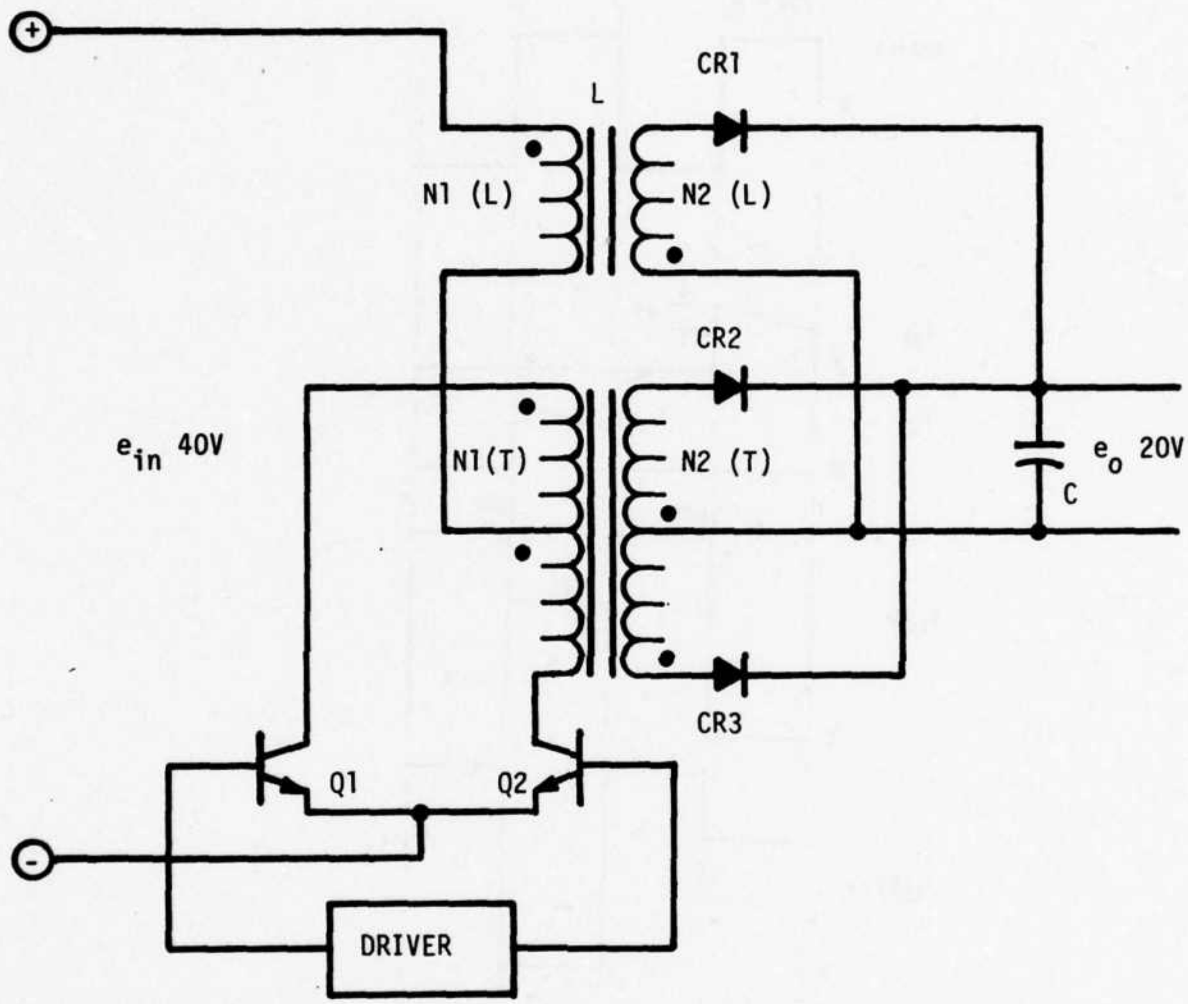
Figure 2-4 presents transformer voltage, inductor voltage power transistor Q1 current and voltage, power transistor Q2 current and voltage and rectifier CR1, CR2 and CR3 current. One complete cycle is present in Figure 2-4, Q1 on, Q1 & Q2 off, Q2 on and Q1 and Q2 off. The example assumes 40 VDC input and 20 VDC output.

When Q1 is on, the 40 volt supply voltage is across the series inductor and power transformer. The change in the power transistor current ΔI is due to the flax swing of inductor L ($E = -L \frac{di}{dt}$). This same current magnitude is flowing in the output diode CR2 to the output load and filter capacitor. The impressed voltages across transistor Q2 is equal to 40 volt ($2 \times E_o$).

When Q1 turns off, the energy stored in inductor L is supplied directly to output filter capacitor through output diode CR1. The impressed voltage across the power transistors is $\underline{E}$ in plus EN1 (L) and equals 60V.

When transistor Q2 is turned on and turned off, the same type of waveform exist as during the transistor Q1 operation.

It is interesting to note the basic difference of the transistor voltages in power stage configuration as compared with a conventional parallel inverter as shown in Figure 2-1. When transistor Q1 is turned on the voltage across Q2 equal $2 \times e_{in}$ vs $2 \times e_o$ as in this configuration. When transistor Q1 is turned off the voltage across Q2 equals e_{in} vs $e_{in} + e_o$ as in this configuration. The net effect is that the peak voltage stress is reduced to 75% of the conventional design configuration



ASSUME N1 (L) = N2(L) & N1(T) = N2T

$e_{in} \approx 40V$

$e_o \approx 20V$

FIGURE 2-3 SCHEMATIC-SERIES INDUCTOR/PARALLEL INVERTER POWER STAGE

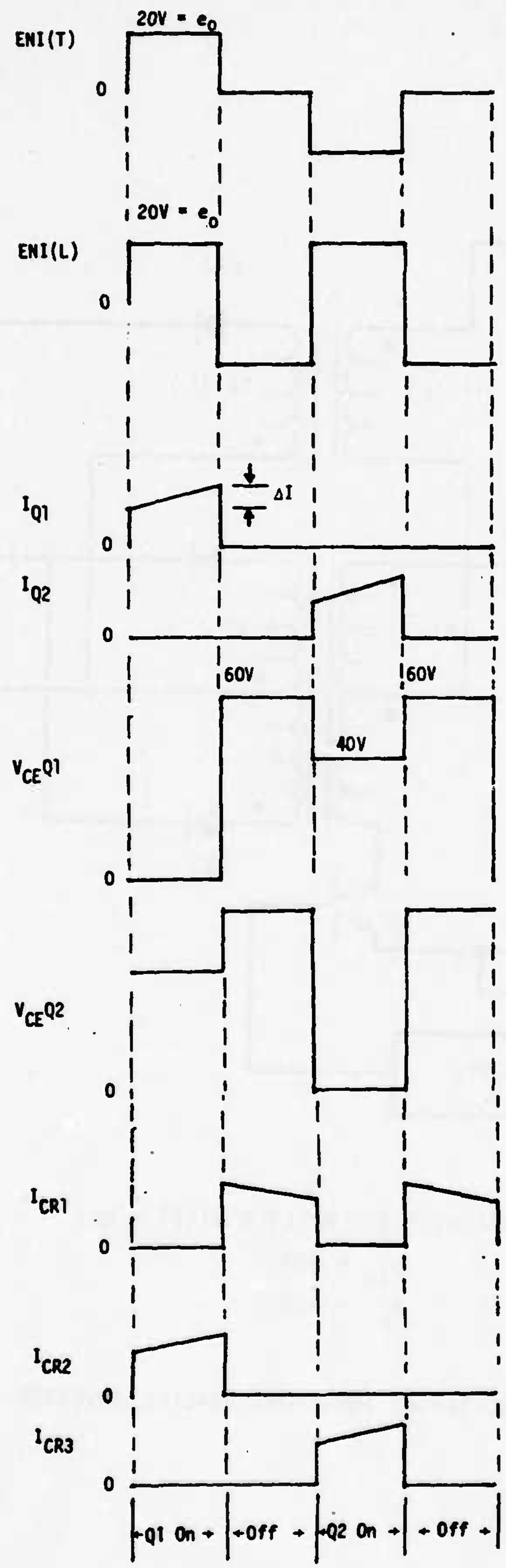


FIGURE 2-4 SERIES INDUCTOR/PARALLEL INVERTER WAVEFORM

The basic advantages of this power stage configuration are (1) lower peak voltage stress on the power transistor (2) the series inductor always provide an impedance in series with power transistor and therefore has inherent current limit during output short, power transformer saturation and overlap of the power transistor Q1 and Q2.

The penalty of the design is that inductor L is about 50% larger due to having two windings instead of one in the conventional circuit and that an additional output diode is required.

The improved reliability due to the reduced voltage stress and current limiting greatly offset the slight increase in the weight of the inductor and the addition of an extra power diode.

The next section will explain in detail the phase displacement, output load sharing and control techniques for output voltage regulation and output current limiting.

3. DEMONSTRATION MODEL

After the completion of the power stage configuration and power semiconductor study, an electrical design was performed and a breadboard was fabricated and tested. The electrical design was packaged into an demonstration model shown in Figure 3-1. The front panel dimensions are 19 inches wide, 12.25 inches high. The main unit dimensions are 11 inches high, 16 inches wide and 18.25 inches long for a volume of 1.86 cubic feet. When the brackets for the cabinet slides are added, the width increases to 17 inches and the volume is 1.97 cubic feet.

The total weight of the demonstration model as shown in Figure 3-1. is 73.3 pounds.

The following section presents a discussion of the DC-DC Converter/ Regulator block diagram, electrical design and mechanical assembly.

FIGURE 3-1 2.4KW DC-DC CONVERTER/REGULATOR DEMONSTRATION MODEL

3.1 Block Diagram

Figure 3-2, presents the block diagram for the 2.4KW DC-DC Converter Regulator.

The input DC power (20-40V) is fed into a input EMI filter, input breaker and input power filter. The DC power goes to four identical series inductor/parallel inverter DC-DC converter power stages each handling 1/4 of the total input power.

The output from each power stage goes to a common output filter, output shunt, output breaker and output EMI filter.

Each power stage includes a series inductor, power transformer and push/pull power transistors. The power transistors are driven by a proportional drive by means of a digital signal from the control logic. The control logic takes signals from feedback control system ring counter, input DC line voltage and instantaneous transformer primary current and generates the correct digital control logic for the push/pull power transistors.

The control logic contains a flip-flop that turns the two power transistors on and off. The on time is initiated by a signal from the ring counter. The turn off is initiated by the volt second control in the control logic or the primary current peak current sensor.

The volt second control senses the input line voltage and allows a constant volt-sec of energy to go into the power inductor and output power transformer. The volt sec control in each power stage module is adjusted during test so that all power modules are carrying 1/4 of the total output power. By this means, no additional electronics are required to cause forced load sharing.

The peak current sensor constantly monitors the power transformer primary current and therefore the power transistor current, and initiates a turn off if the instantaneous peak current is beyond a threshold limit. This provides inherent transistor protection during all transients and steady state modes of operation.

A common output voltage regulator and voltage divider/remote sense network monitors the output dc voltage and in conjunction with the AC signal from the output filter determines a output voltage to the voltage to frequency oscillator that commands the turn-on of the four separate phase displaced power modules through the ring counter.

The net output voltage of the error amplifier provides a voltage level to voltage to frequency oscillator which is the heart of this control system in that all power modules are operating at the same frequency. The oscillator operating frequency is proportional to the input amplified error voltage.

The power module phase displacement is controlled by the ring counter which sends sequential pulses to each of four power modules to initiate power transistor turn on.

The signal from the output shunt and current regulator overrides the voltage regulator and reduces the overall operating frequency of the voltage to frequency oscillator during overload operations. Front panel adjustments are provided to allow for the 24 to 32Vdc output voltage adjustment and for the 0 to 75A output current limit.

The output of the voltage to frequency oscillator passes through an optical isolator that isolates the output power ground from the input power ground and commands the ring counter to provide the correct duty cycle of the four separate power modules.

An undervoltage/overvoltage sensor monitors the DC input power and can inhibit the ring counter operation during abnormal input line conditions (less than 20V and greater than 40Vdc).

The front panel meter can monitor the DC output voltage or DC output current.

Control electronics power is obtained from the main DC input through a fuse to a control electronics DC-DC converter. The control electronics DC-DC converter provides +10V and +5V output which is common with the input power ground and two isolated +10V outputs for the output voltage and current regulators.

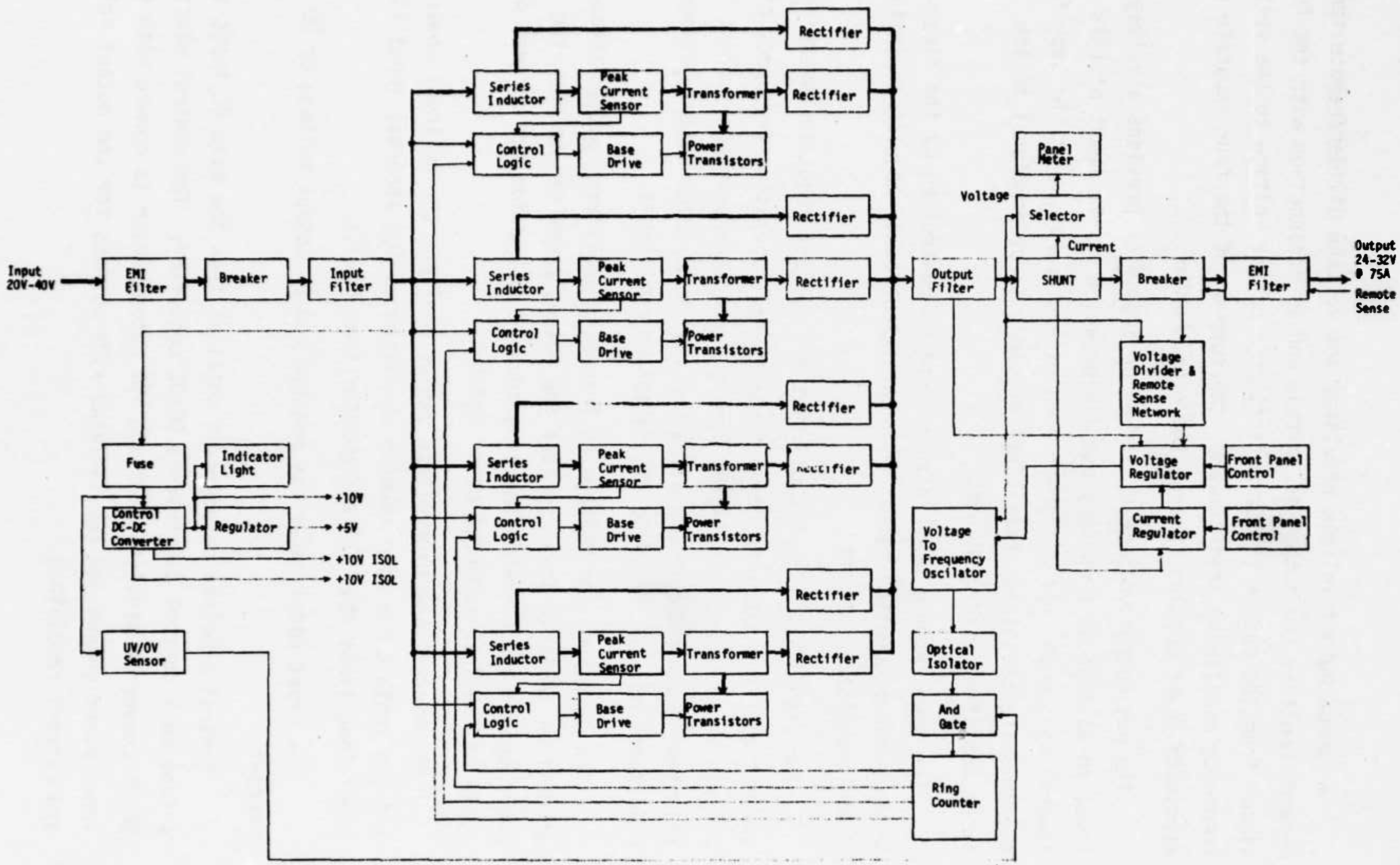


FIGURE 3-2 BLOCK DIAGRAM FOR 2.4KW DC-DC CONVERTER/REGULATOR

3.2 Electrical Design

The electrical design is contained in the following schematics:

Figure 3-3, Input Filter and Front Panel Control
Figure 3-4, Output Filter and Measurement Circuit
Figure 3-5, Power Stage
Figure 3-6, Drive Amplifier
Figure 3-7, Control Electronics

The schematics also contain the interconnections between schematics and the relative location of the component.

A1 - Front Panel
A2 - Rear Panel
A3 - Left Heat Sink
A4 - Right Heat Sink
A5 - Center Filter Capacitor Assembly
A6 - Control Electronics Printed Circuit Card

3.2.1 Input Filter and Front Panel Controls

Figure 3-3 contains the schematic of the Input EMI Filter, the Primary Power Circuit Breaker (CB1) and the Two Stage Input Filter. The first stage filter includes inudctor L1 and capacitors C1 and C2. The internal resistance of C1 and C2 control the first stage resonance. The second stage filter includes inductors L2 and L3 and shunt resistors R2 and R3 to control resonant peak. The second stage capacitors are located on the two side power modules.

The shunt diode CR1 protects the DC-DC converter if input power is connected in reverse mode and also protects the contacts on breaker CB1 from the input filter discharge during turn off.

The schematic also contains the fuse for control electronics power, the indicator light and the output voltage and current adjustment.

Appendix A presents the detailed parts list for the 2.4kW DC-DC Converter/Regulator.

Input Power 0-40VDC, 0-150A

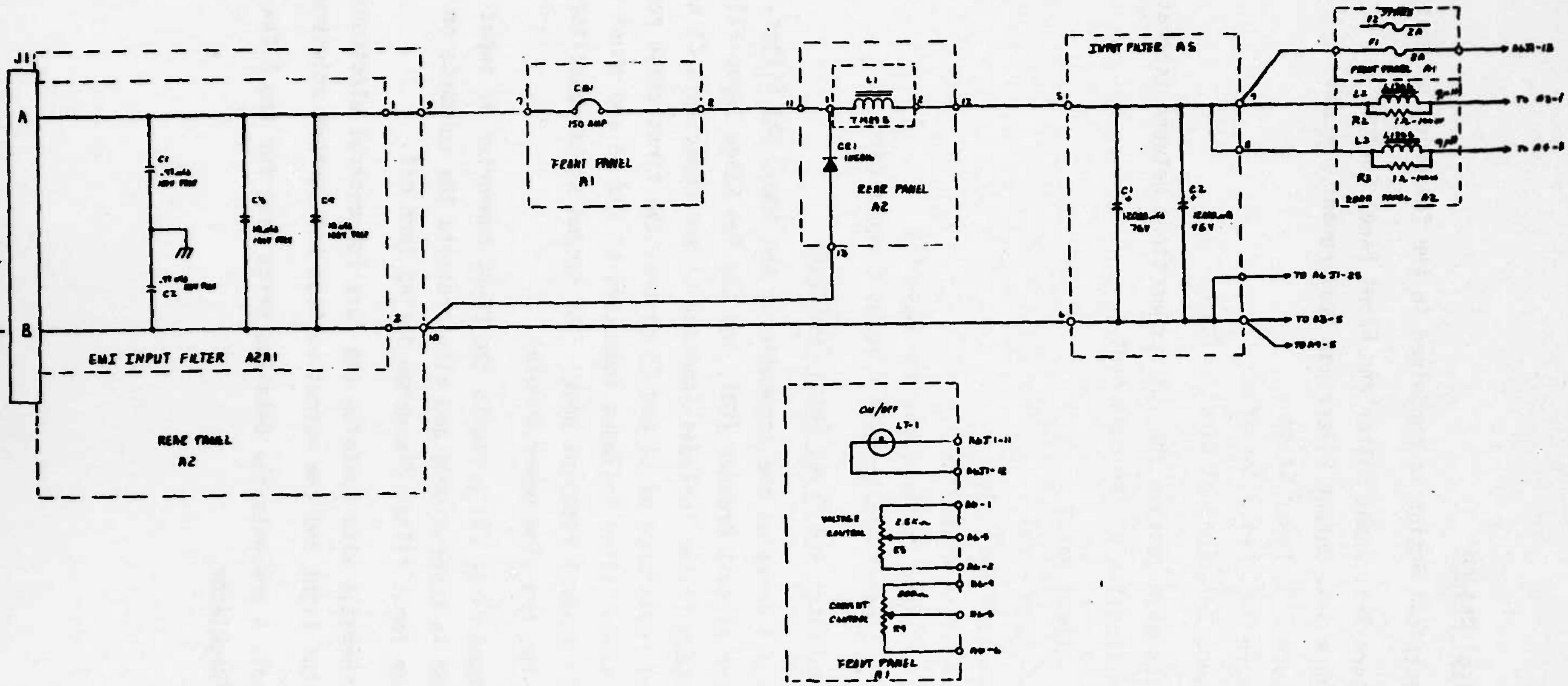


FIGURE 3-3 SCHEMATIC-INPUT FILTER AND FRONT PANEL CONTROL

3.2.2 Output Filter and Measurement Circuit

Figure 3-4 contains the schematic for the output filter and measurement circuit. The output includes capacitors C3 and C4. Transformer T1 senses the energy change in the output filter and is used for the feedback loop stability compensation.

The output EMI filter is shown for the main power line and remote output sensing lines.

The remote sense transfer network consists of resistors R1 and R2.

The meter M1 is used to monitor output voltage or output current across shunt R1 located on the rear panel A2. The voltage across the shunt is also used for current limiting in the control electronics.

3.2.3 Power Stage

Each side heat sink includes two power stages and its associated drive amplifiers.

Figure 3-5 presents the schematic of the four power stages. The power stage includes two sets of parallel power transistors Q1-Q2 and Q3-Q4 operating in push-pull operation in a parallel inverter configur-ation. The module input capacitor C1 & C3 form the second stage input filter network shown in the input filter network.

Zener VR1 limits the maximum peak voltage that can appear across the power transistor collector emitters.

The power magnetic assembly T1 include the series inductor (T1562A), power output transformer (T1527A) and peak current sense transformer (T1471A).

The output from the inductor and power transformer is rectified by diodes CR1 and CR2. Local energy storage is provided by capacitor C2 and C4. The output of the current sense transformer is used for instantaneous protection of the power transistors by means of the control logic.

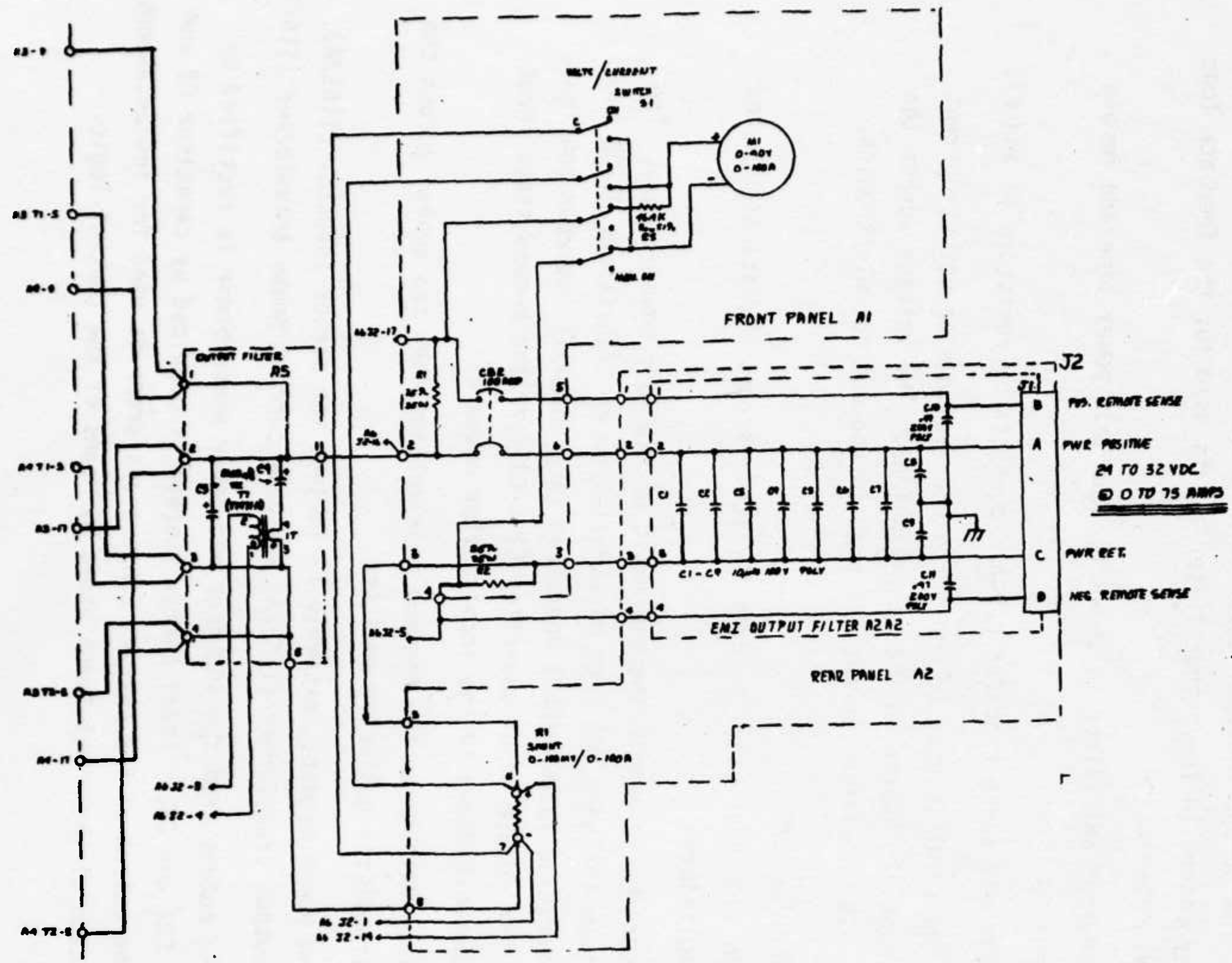


FIGURE 3-4 SCHEMATIC-OUTPUT FILTER AND MEASUREMENT CIRCUIT

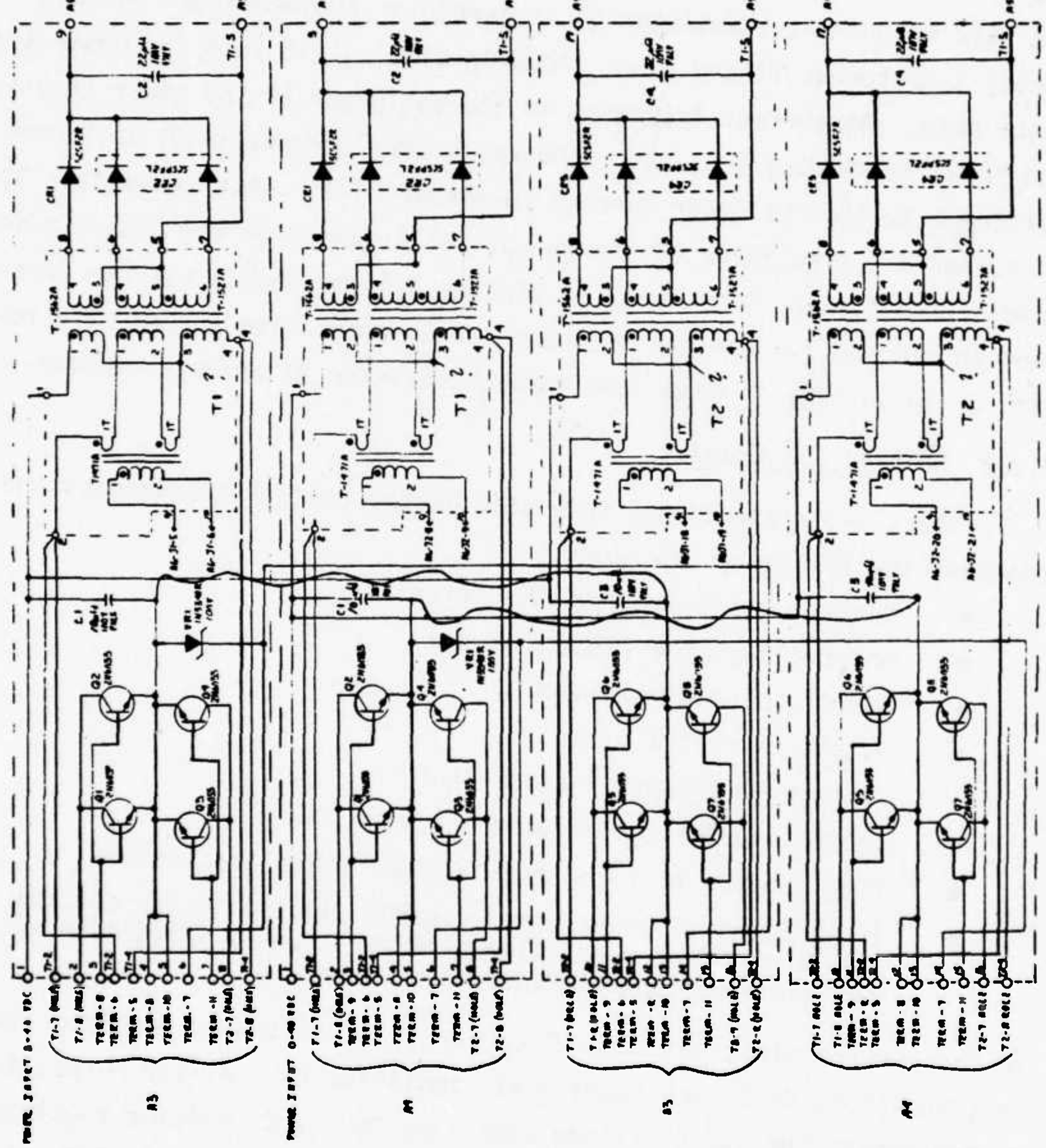


FIGURE 3-5 SCHEMATIC-POWER STAGE A3 & A4

3.2.4 Drive Amplifier

Figure 3-6 presents schematic of the drive amplifier. The drive amplifier includes two proportional base drive transformers T1 and T2 and the drive transistor Q1 through Q4. When Q3 is turned off by shorting the base to ground, transistor Q1 is turned on and developes voltage across transformer T1 and power flows in winding 1-2 into the power transistor base. As current increases in the collector of the power transistors and flows in winding 7-8, this provides a base current in Q1 to be proportional to the collector current in winding 1-2. When transistor Q3 is turned on, transistor Q3 shorts out the drive to Q1 and places a short across transformer T1 by means of winding 3-4 and shorts out the current flow in winding 1-2. After the power transistors have turned off, reverse bias drive voltage is generated through resistor R7 through winding 3-4.

3.2.5 Control Electronics

Figure 3-7 presents the schematic of the control electronics and contains the following functions:

- Control electronics DC-DC converter
- Undervoltage/overvoltage sensor
- Output voltage regulator
- Output current limiter
- Voltage to frequency oscillator
- Input/output signal ground isolator
- Ring counter to turn on each power stage electronics
- Four identical power stage control electronics to control the pulse width modulation as a function of input line and instantaneous power transistor current.

In the control electronics DC-DC Converter, a switching regulator is formed by transistors Q1-Q3 and operational amplifier U1. A +10V output is generated across the output filter capacitor C6. I.C. voltage regulator U2 generates a +5V output from the +10V output. Two isolated +10V outputs are obtained from the output filter inductor L1.

The undervoltage sensor is U6 and the overvoltage sensor is U5 and turns the control electronics off below 20Vdc and above 40Vdc input. Operational amplifier U4 is the voltage regulator.

The AC signal from the output filter capacitor for the ASDTIC control is fed to the network CR4, CR5, R21 and amplifies U4.

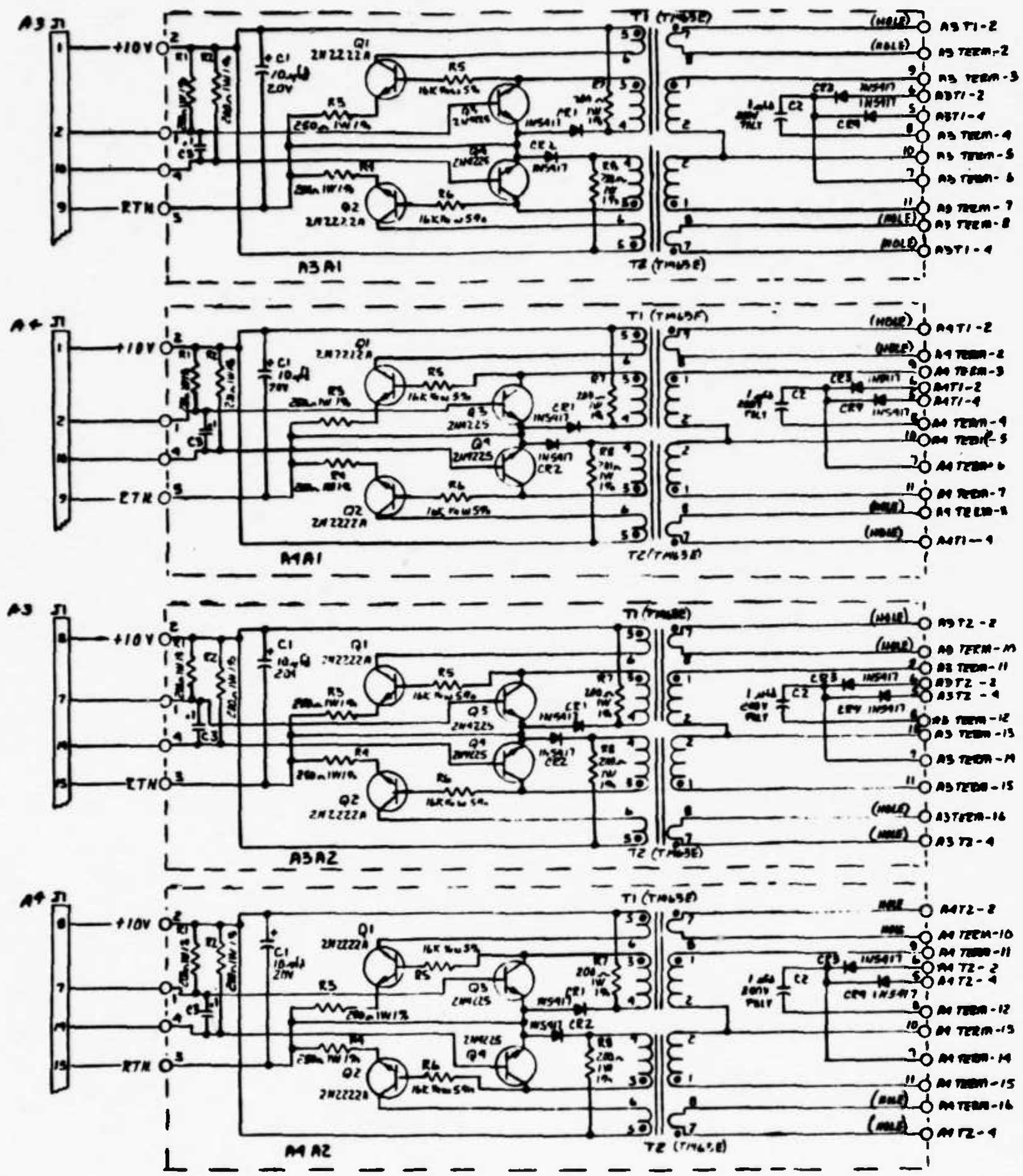
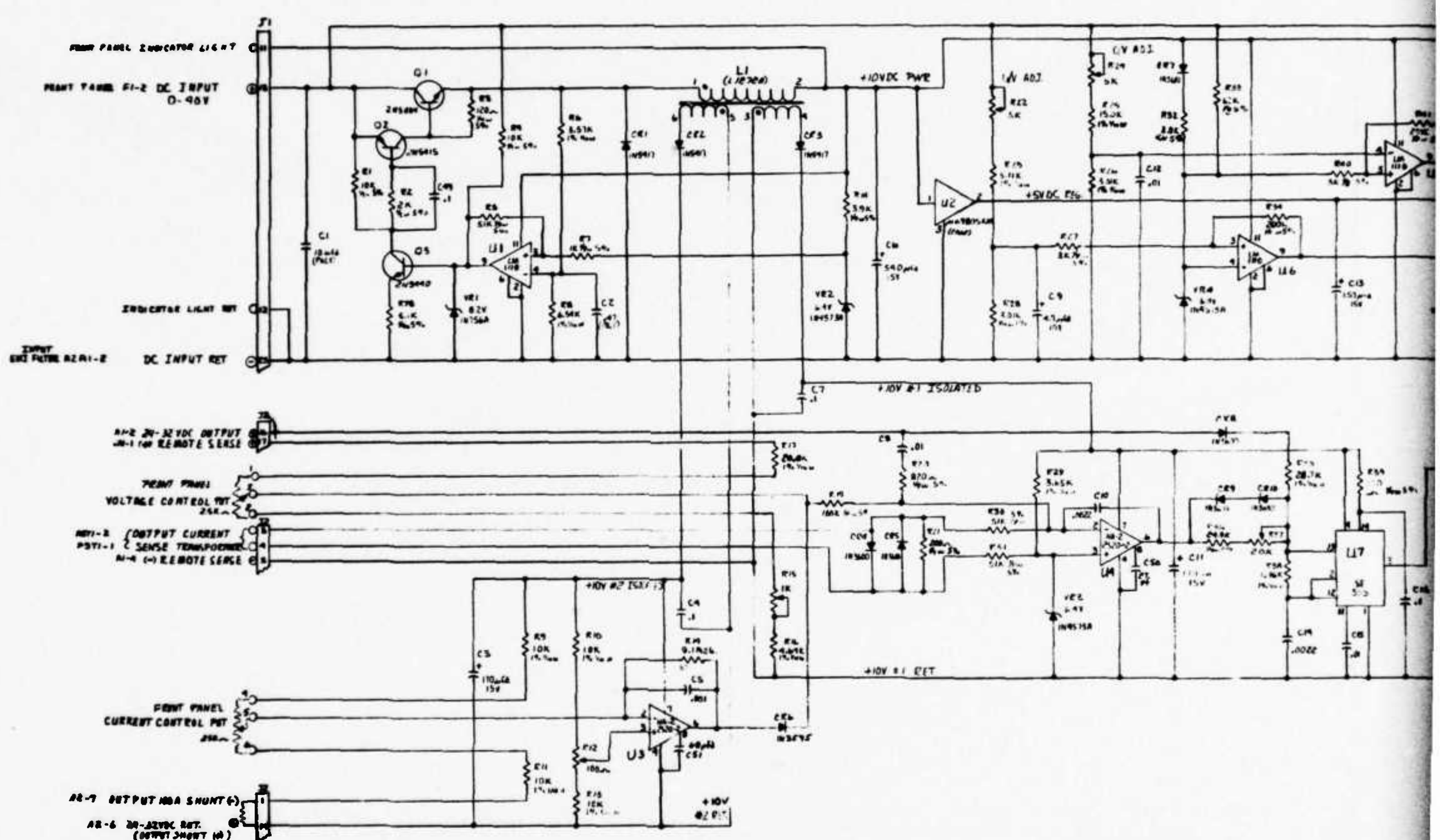


FIGURE 3-6 SCHEMATIC-DRIVE AMPLIFIER



J1
FRONT PANEL INDICATOR LIGHT
FRONT PANEL F1-2 DC INPUT
0-40V
INDICATOR LIGHT RET
DC INPUT RET
L1
+10VDC PWR
U2
U1
U3
U4
U6
U17
+10V #1 ISOLATED
+10V #1 RET
+10V #2 ISOLATED
FRONT PANEL
VOLTAGE CONTROL POT
FRONT PANEL
CURRENT CONTROL POT
+10V
#2 RET

1

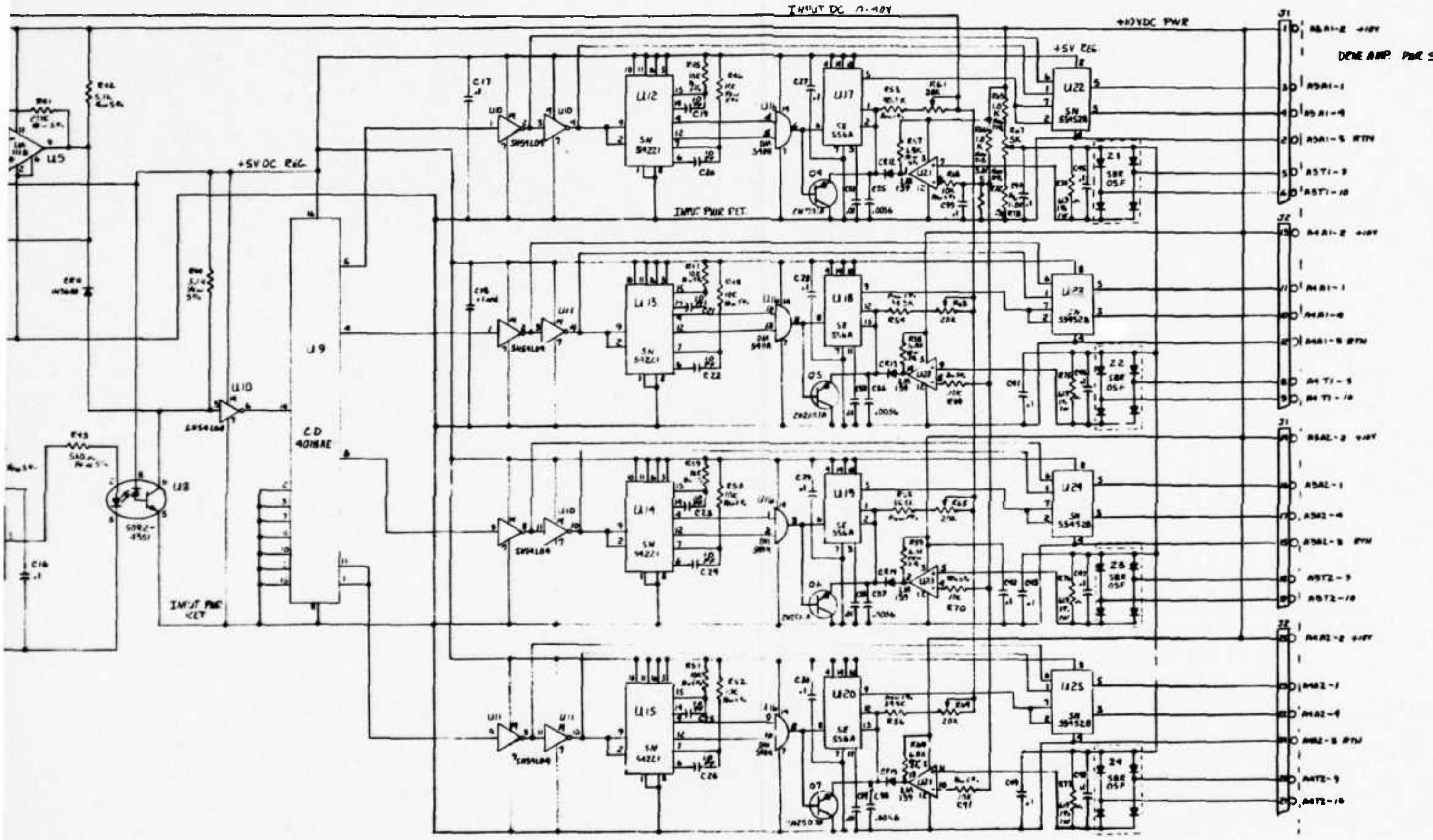


FIGURE 3-7 SCHEMATIC-CONTROL ELECTRONICS

2

Operational amplifier U3 is the output current limiter and its output is fed into the voltage regulator U4.

The output from the voltage regulator U4 goes into the voltage to frequency oscillator U7 whose output frequency is proportional to the error input voltage from U4.

The optical isolator U8 passes digital signals from the output ground to the input ground, thereby providing the necessary ground isolation in the control electronics and output power from the input power lines.

The digital signals from U8 pass through the gate U10 PIN 5 and into the ring counter U9. Outputs from the undervoltage sensor U6 and overvoltage sensor U5 are inhibited by U10 PIN 5 and stops any pulse information from U8 to pass into the ring counter U9.

Four separate signals are obtained from U9 (ring counter) to operate the four separate power stage control electronics and provides the necessary phase displacement.

The power stage control electronics are the same for all stages and therefore only one stage of control electronics will be discussed. Driver amplifier U22 provides the necessary digital signals to the proportional drive system discussed in Figure 3-6.

The on-time of the drive amplifier U22 is controlled by the timer U17 and the voltage on its timing capacitor C35. The normal on-time is determined by the charging resistors R53 and R61 and the input line voltage. This RC time constant is proporational to input line voltage and gives a constant voltage of energy to the power stage inductor and power transformer. R61 - R64 is the timing adjustment for each respective power stage.

At the beginning of each half cycle, the monostable multivibrator U12 generates a 0.1μs pulse that resets the timer U17 and its timing capacitor C35 through transistor Q4.

When currents flow in the power transistors of the power stage, a voltage is generated across resistor R74. This voltage is compared in the voltage comparator U21. If the voltage value is greater than

the reference value, an output is generated which causes the timing capacitor C35 to be charged up faster thereby terminating the on-time pulse during that particular half cycle. This circuit provides instantaneous peak current protection for the power switching transistors. Adjustment is provided by resistor R67.

This demonstrates the volt-second control of the electronics and the peak current sensing action.

3.3 Reliability Prediction

A reliability prediction was performed on the DC-DC converter module based on MIL-HBK 217B. Table 3-I presents the part types, failure rate, quantity of components and total failure rate. The analysis shows a 8265 hour mean-time between failure and exceeds the 5000 hour MTBF contract goal.

TABLE 3-I DC-DC CONVERTER/REGULATOR RELIABILITY PREDICTION

Part Type	Failure Rate Per 10^6 Hr.	Quantity	Total Failure Rate Per 10° Hour
Diode Power	.9	9	8.1
Signal	.68	35	23.8
Zener	.85	6	5.1
Transistor	.9	39	35.1
Magnetic Power	.034	12	.4
Signal	.0045	9	.04
Cap. Elec.	.11	4	.4
Poly.	.0012	25	.03
Mia/Ceramic	.06	60	3.5
Tant.	.052	9	.47
Resistor Power	.18	4	.72
Film	.042	23	.97
Carbon	.0085	76	.65
Pot	8.5	2	17.0
Trim Pot	.9	10	9.0
I.C.	1.2	24	28.8
Connector	1.0	2	2.0
Breaker	.5	2	1.0
Switch	.1	1	.1
LT	.2	1	.2
Meter	.5	1	.5
Fuse Holder	.1	1	.1
Shunt	.0085	1	.008

Total Failure Rate 121 bits/10^6 hour

Mean time between failures (MTBF) 8265 hours

3.4 Mechanical Assembly

The demonstration model of the 2.4kW DC-DC Converter Regulator, shown in Figure 3.1, is divided up into nine electrical/mechanical subassemblies:

A1	Front Panel (Breakers & Meter and Control)
A2	Rear Panel (Connectors, EMI Filters, Input Inductor and Output Shunt)
A3 & A4	Side Panels (Identical Two Power Modules on Each)
A5	(Center Bracket Input/Output Filter Capacitors)
A6	Control Card
A7	Mounting Frame & Thermal Barrier
A8 & A9	Top and Bottom Covers

Figure 3-8 shows the open view of DC-DC Converter/Regulator which allows electrical checkout.

Figure 3-9 shows the front panel (A-1). It has a dimension of 12.25 inch high and 19 inch wide, it contains the input breaker, indicator light, control power fuse, output breaker, output voltage and current adjustments and the output meter and its selector switch. The input controls are grouped at the left and the output controls are grouped on the right.

Figure 3-10 shows the rear panel (A-2) with input connector (Top) and output connector (Bottom).

Figure 3-11 shows the side panels (A-3 power stage). It is the same for other panel A-4. It contains two series inductor parallel inverter power stages each.

The A5 module is shown in the center of Figure 3-8. It contains the input filter capacitor on its front side and the output filter capacitors on the rear side.

Figure 3-12 shows the printed circuit board (A-6) for the low level control electronics. It can be removed from the bottom of the demonstration model.

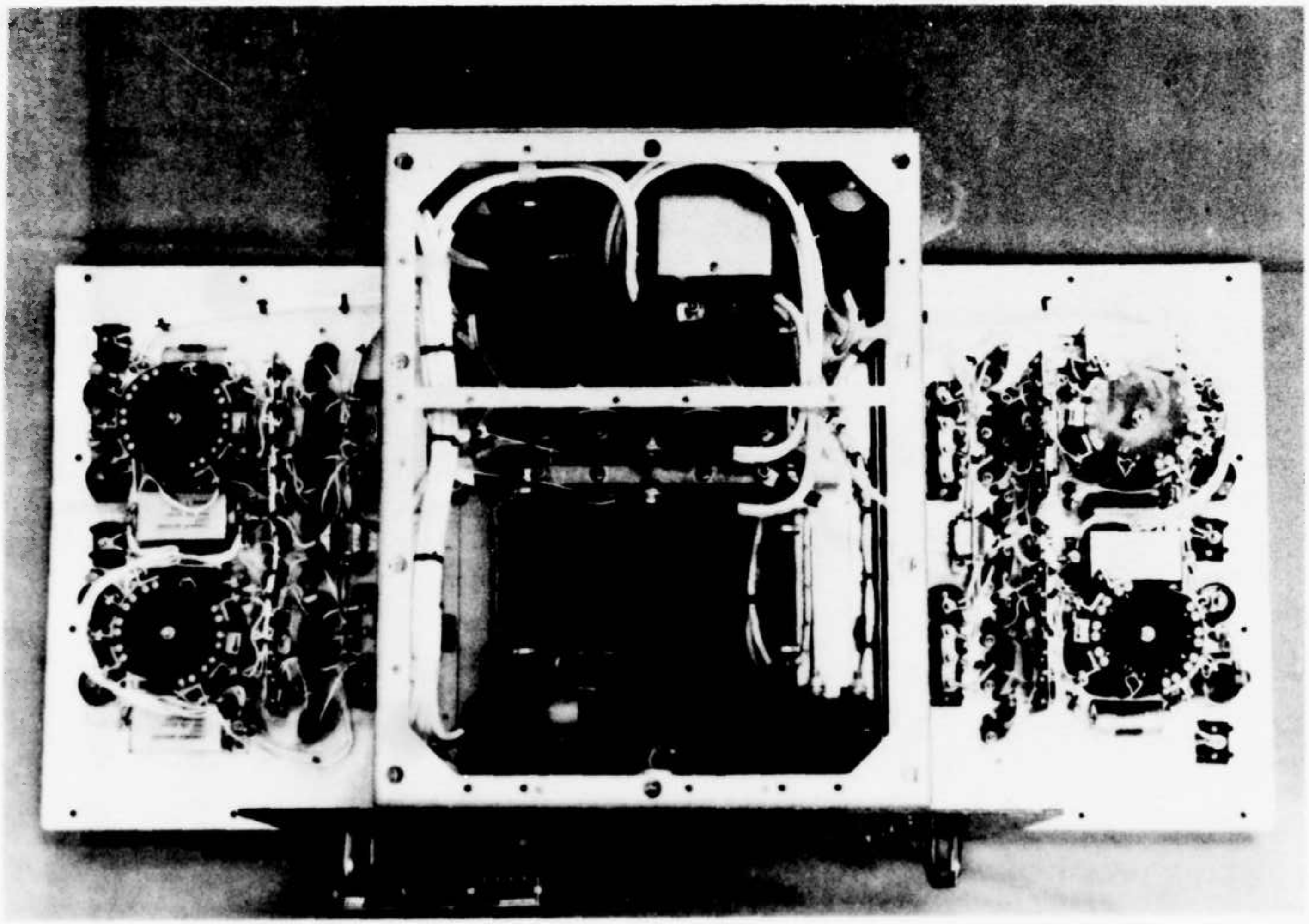


FIGURE 3-8 TOP VIEW OF DC-DC CONVERTER/REGULATOR

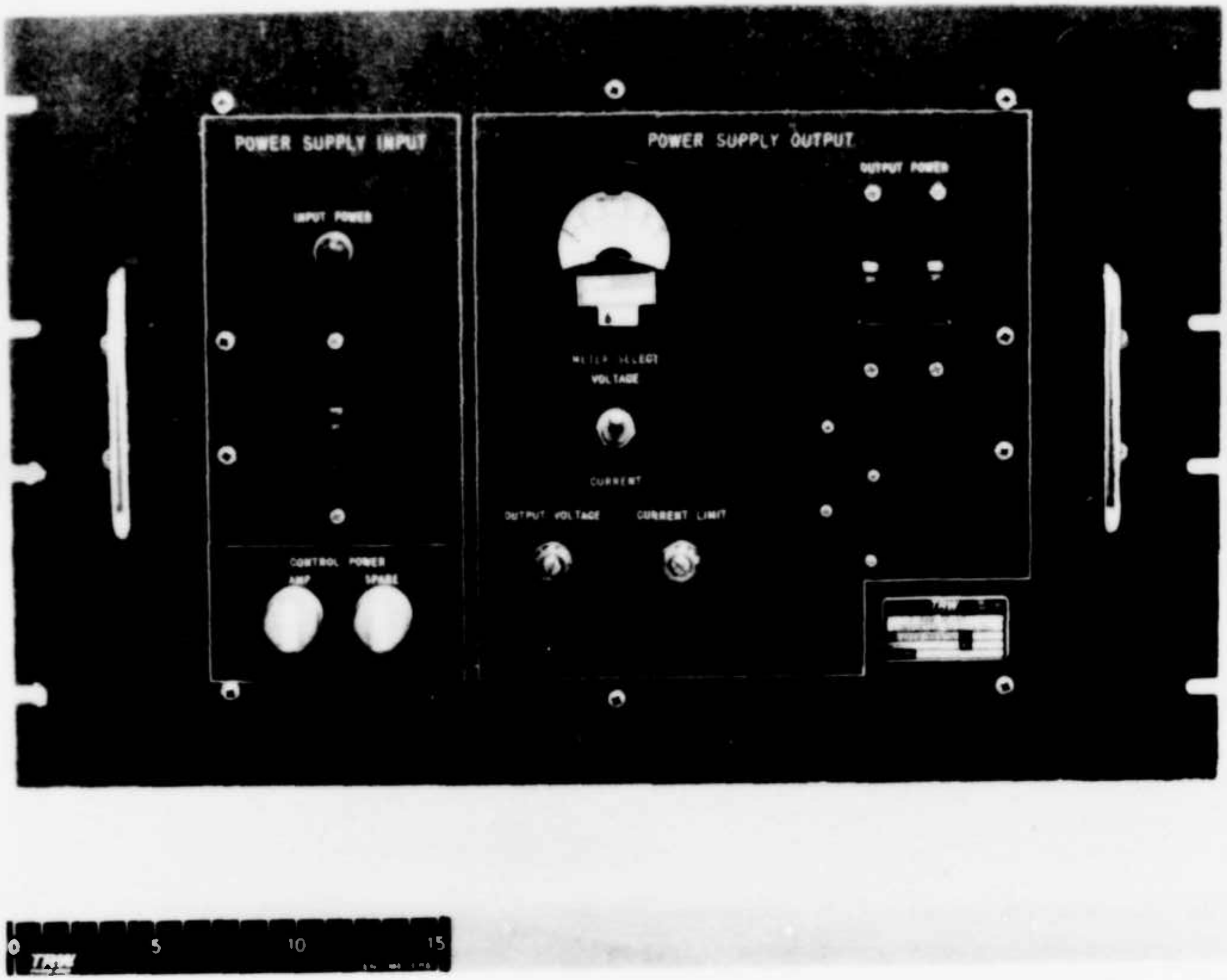


FIGURE 3-9 FRONT PANEL VIEW

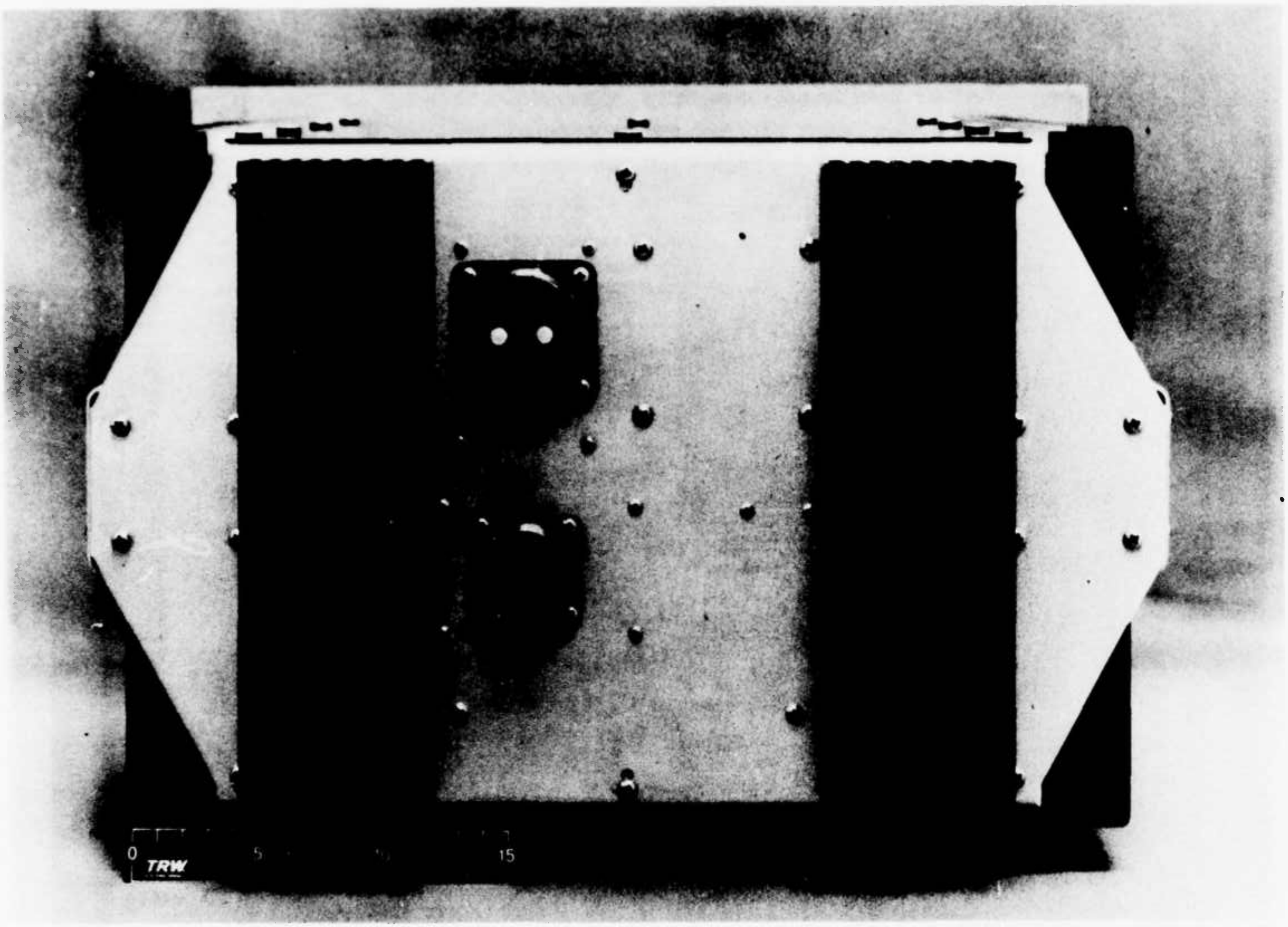


FIGURE 3-10 REAR PANEL VIEW

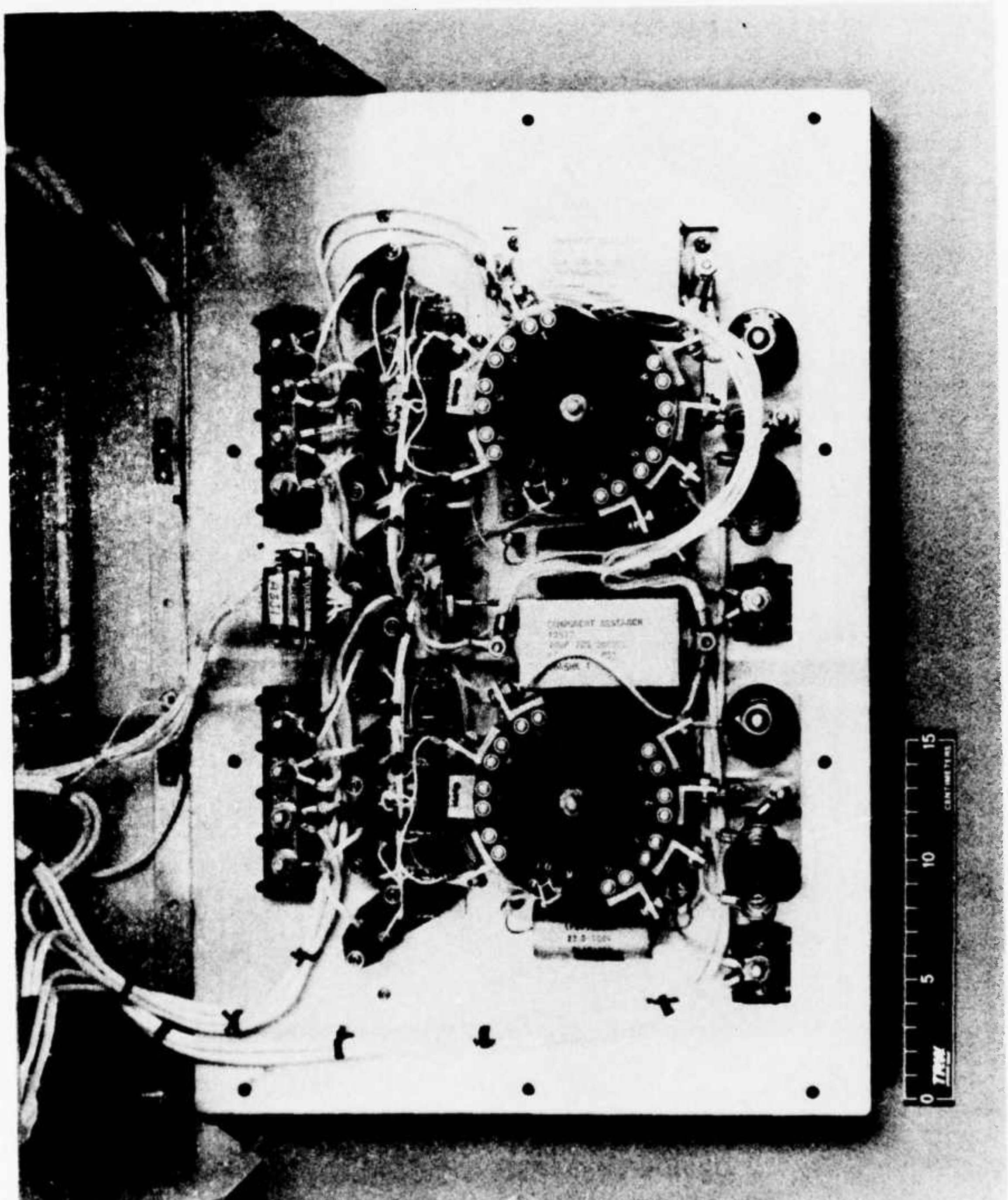


FIGURE 3-11 POWER MODULE VIEW (SIDE PANEL)

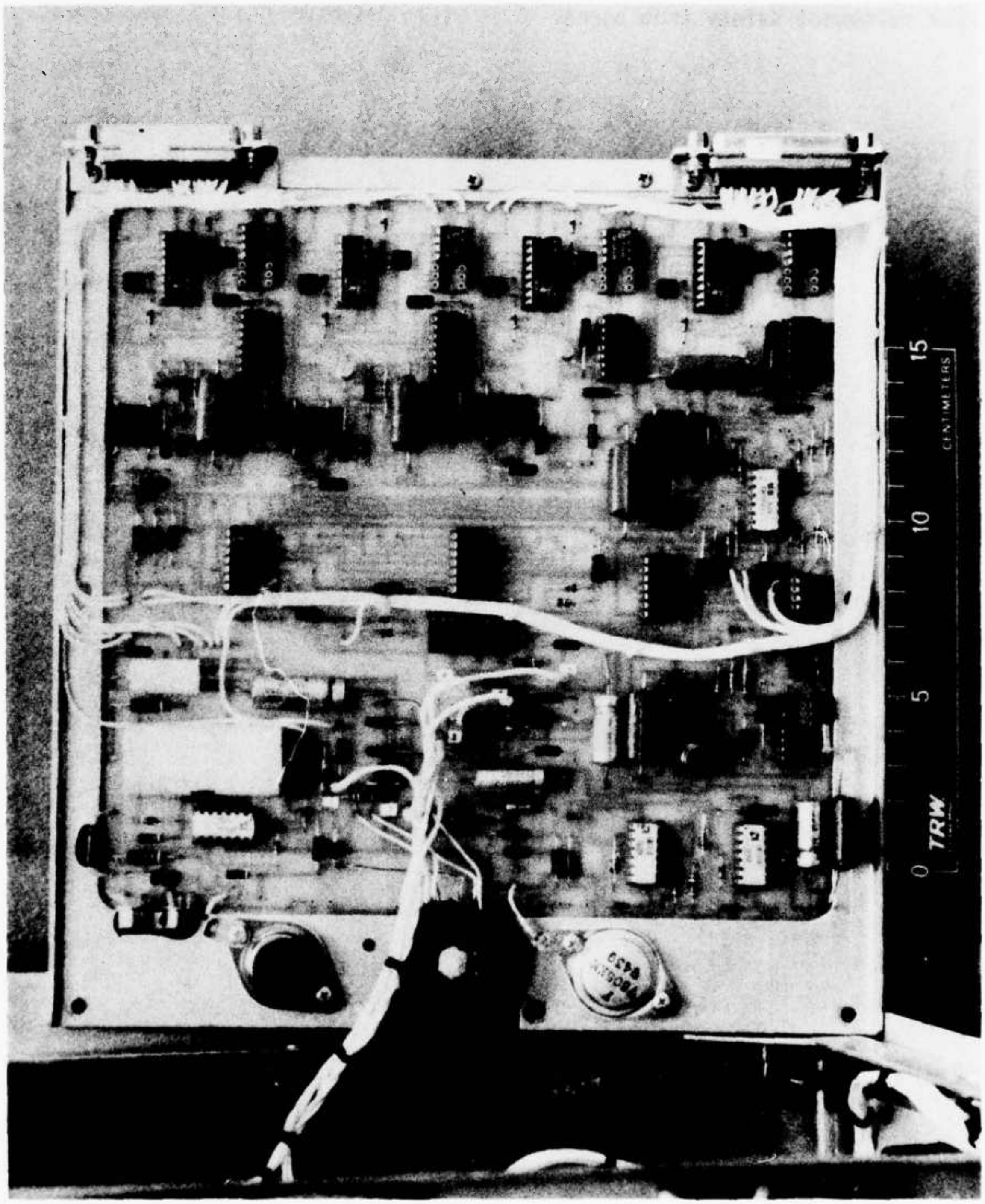


FIGURE 3-12 PRINTED CIRCUIT BOARD FOR CONTROL ELECTRONICS

All heat producing components are located on A-2, A-3 and A-4 assemblies. The front panel A-1 does not have any heat producing component to allow the front panel to be maintained at low temperatures for personnel safety from burns.

4. TEST RESULTS

The DC-DC converter/regulator demonstration model was fully tested. The following sections summarizes the test results and is grouped into the following four sub-sections:

- Electrical Performance
- Thermal Control
- Electromagnetic Interference
- Acoustic Noise

4.1 Electrical Performance

The electrical performance test results include:

Line voltage regulation
Load current regulation
Output ripple
Output current limit
Battery charging
Undervoltage/Overvoltage protection
Output regulation due to ambient temperature
Remote sense regulation
Efficiency
Step load transient response
Continuous 72 hour operation

Table 4-I presents the test summary of the output regulation due to input line voltage changes from 20VDC to 40VDC.

Table 4-II presents the test summary of the output regulation due to output load current variation from 0 to 75A. The dual loop feedback system (ASDTIC) allows the output voltage regulation error to be extremely small without any feedback control system instabilities.

Table 4-III presents the output ripple data at the different output voltage settings and load currents. The output ripple value exceeds the specification goal of 50mV RMS.

Table 4-IV presents the current limit regulation data for output current limiting setting at 5A, 25A and 75A. The maximum current regulation is less than 1A. The DC-DC converter/regulator was operated with a lead calcium battery bank both during the current limit mode and voltage limit mode. No output instability was noted during the battery charging mode.

Table 4-V presents the data on the undervoltage and overvoltage turn off of the unit. Both the IR drop between the power source and demonstration model and power source dynamic response influence the exact reading. The unit has adjustments for the voltage setting but the setting hysteresis is fixed. This hysteresis should be adjusted to be compatible with the power source and cabling characteristics.

TABLE 4-I

OUTPUT REGULATION DUE TO LINE CHANGE

e_o	ΔE_o (e_{in} 20 to 40V)
24V	6mV
28V	12mV
32V	16mV*

*Note: Input line variation was 22 to 40Vdc during this test.

TABLE 4-II

OUTPUT REGULATION DUE TO LOAD CHANGE

e_o	ΔE_o (I_o 0 to 75A)
24	2mV
28	3mV
32	4mV

TABLE 4-III OUTPUT RIPPLE

	Ripple P-P (e_{in} = 28V)		
I_o Amps	e_o = 24V	e_o = 28V	e_o = 32V
0	50mV	20mV	20mV
5	20mV	20mV	30mV
25	40mV	40mV	50mV
50	70mV	70mV	70mV
75	80mV	80mV	100mV

TABLE 4-IV CURRENT LIMIT REGULATION

I_o Set 5A		I_o Set 25A		I_o Set 75A	
ΔE_o	ΔI_s	ΔE_o	ΔI_s	ΔE_o	ΔI_s
28-70	0.28A	28-70	.98A	28-70	.83A

Table 4-VI presents results of demonstration model output voltage regulation due to line, load and ambient temperature variation.

Table 4-VII presents output voltage regulation with the demonstration model operating in the remote sense mode. When the remote sense line is open the unit automatically transfers to internal local sense for output voltage regulation.

Figure 4-1 through 4-3 presents the power efficiency of the demonstration model for $e_o = 24V$, $e_o = 28V$ and $e_o = 32VDC$. Efficiency is shown as a function of output current and as a function of input DC voltage of 28V, 28V and 40VDC. The no load standby losses are less than 13W at maximum input line.

Figure 4-4 presents the output transient response when the output is switched between 0 and 75A (No load - full load). Figure 4-5 presents the output transient response when the output is switched between 33 and 75A (half load - full load).

In Figure 4-4a, the output voltage deviation is 2V when going from no load to full load. In Figure 4-4b the output deviation is 0.6V when going from full load to no load.

In Figure 4-5a, the output voltage deviation is 0.8V when going from half load to full load. In Figure 4-5b the output voltage deviation is 0.15V when going from full load to half load.

These transient response photo's demonstrate the good dynamic response generated by the application of the dual loop feedback control system that is used for the output voltage regulation.

Table 4-VIII presents the data obtained during the continuous 72 hour operation. After the first two hours the output voltage deviation was 2mV. Operating temperature data of the demonstration model was taken during this test and is presented in Section 4.2 Thermal Control.

TABLE 4-V UNDERVOLTAGE/OVERVOLTAGE PROTECTION

Operation Mode	E_{IN}
Normal e_o = 28V I_o = 75A	28V
Undervoltage Turn Off	18.9
Undervoltage Turn On	19.420
Overvoltage Turn Off	47.85
Overvoltage Turn On	40.045

TABLE 4-VI AMBIENT TEMPERATURE REGULATION

Output Voltage Regulation due to Ambient Temperature of 0°F to 120°F

e_o	ΔE_o e_{in} = 20-40V T_A 0°F to 120°F I_o = 0-75A
24	47mV
28	16mV
32	34mV

TABLE 4-VII REMOTE SENSE REGULATION

Remote Sense Regulation at e_o = 28V/ e_i = 28V

Test Condition	Output Deviation
Load regulation (0 - 75A)	6mV
Temperature regulation (0°F-120°F)	6mV

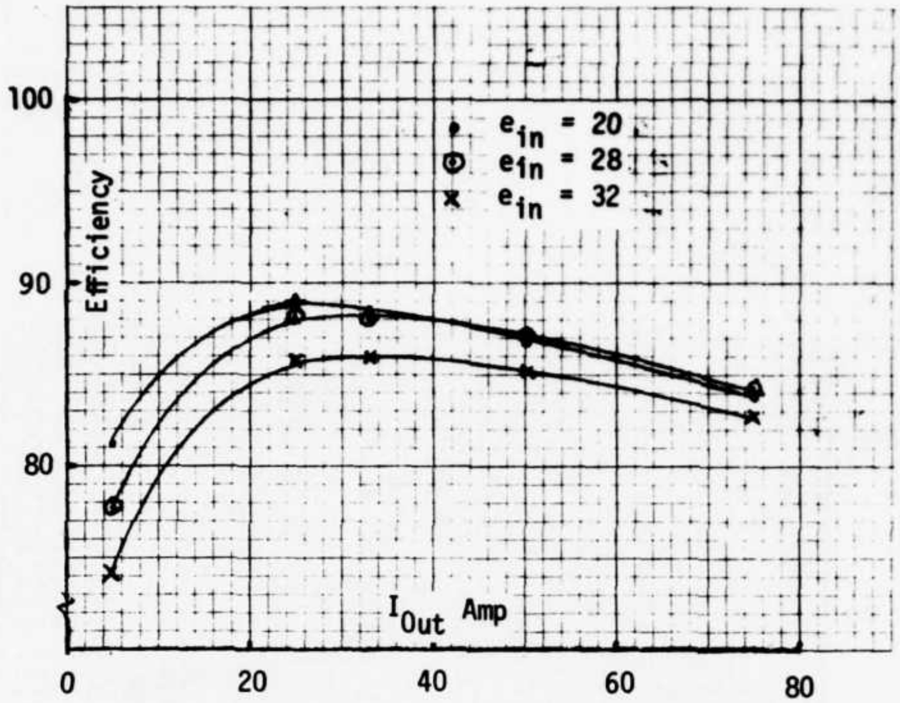


FIGURE 4-1 OUTPUT EFFICIENCY AT e_o = 24V

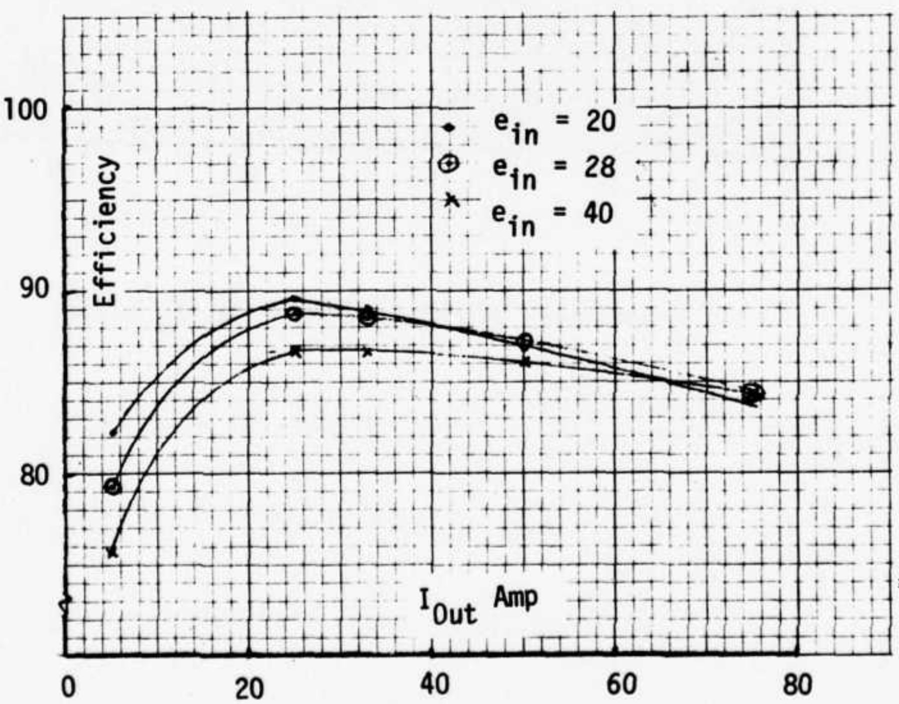


FIGURE 4-2 OUTPUT EFFICIENCY AT e_o = 28V

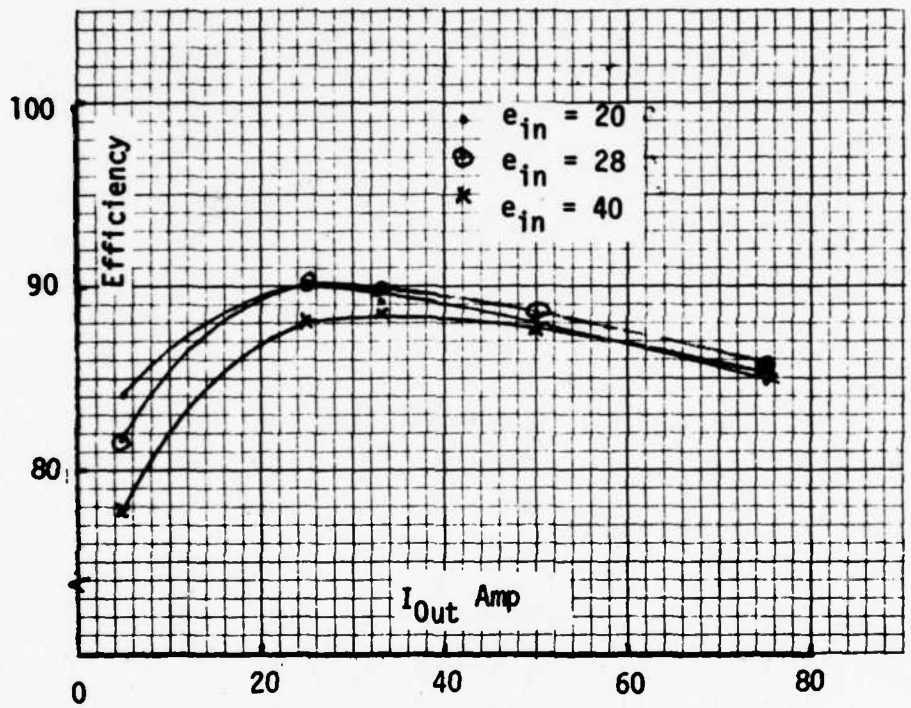
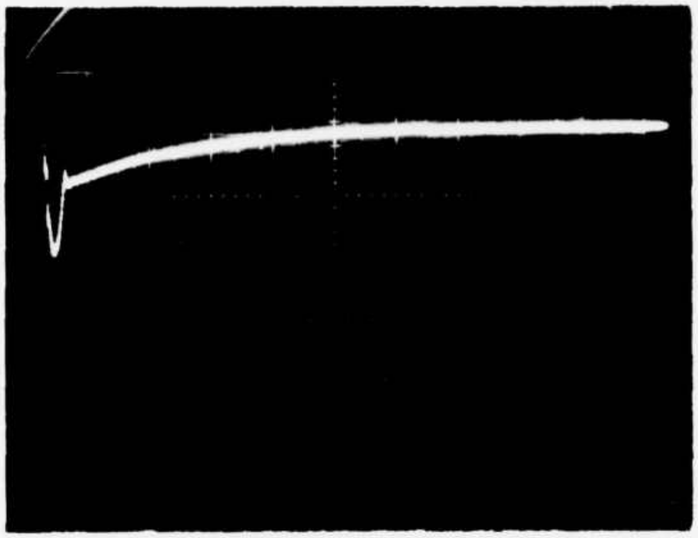
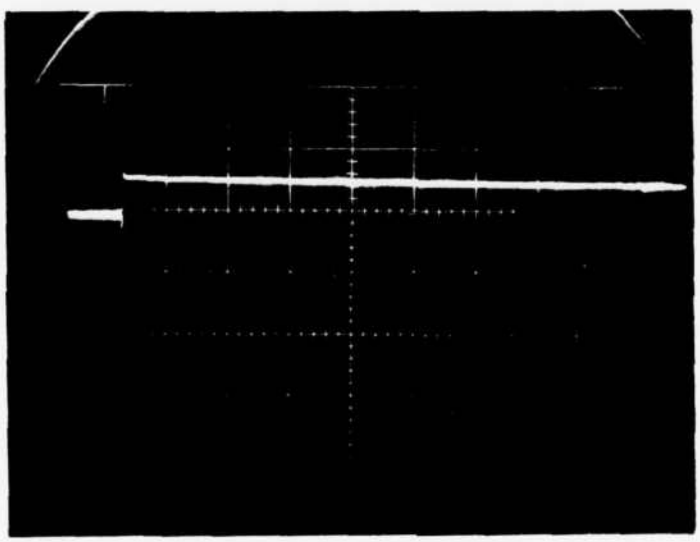


FIGURE 4-3 OUTPUT EFFICIENCY AT e_o = 32V



Scale
1V/Div
5ms/Div

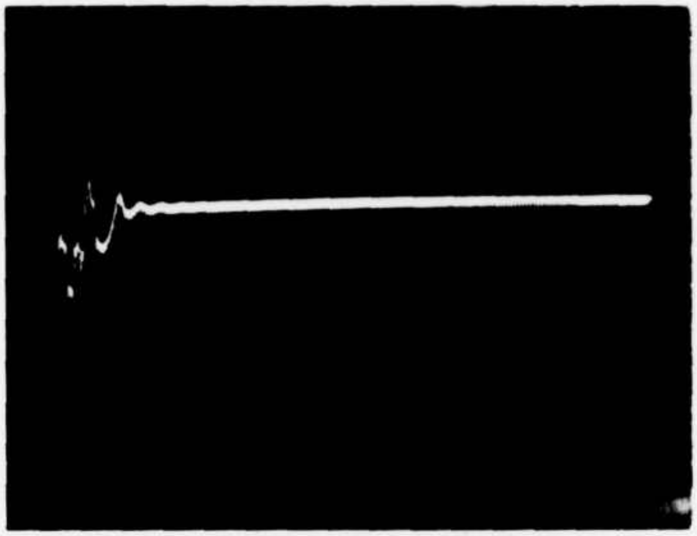
a) No Load to Full Load



Scale
0.5V/Div
20ms/Div

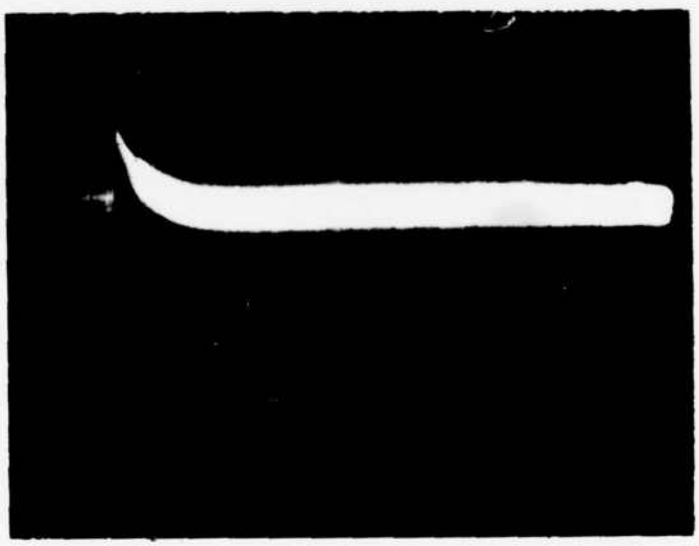
b) Full Load to No Load

FIGURE 4-4 OUTPUT STEP LOAD TRANSIENT RESPONSE (NO LOAD-FULL LO



Scale
0.5V/Div
2ms/Div

a) Half Load to Full Load



Scale
0.1V/Div
20ms/Div

b) Full Load to Half Load

FIGURE 4-5 OUTPUT STEP LOAD TRANSIENT RESPONSE (HALF LOAD-FULL LOAD)

TABLE 4-VIII STABILITY AND CONTINUOUS OPERATION

	INPUT			OUTPUT			
Time	E_{IN}	$I_{IN} \times 2$	P_{IN}	E_0	I_{OUT}	P_{OUT}	LOSSES
0 Hr	28.180	43.86	2472	28.013	75.54	2116	356
2 Hr	28.085	44.58	2504	28.030	75.08	2104	400
5 Hr	28.010	44.80	2509	28.030	75.03	2103	406
8 Hr	27.970	44.87	2510	28.031	75.01	2103	407
24 Hr	27.859	44.88	2510	28.032	75.04	2103	406
48 Hr	27.941	44.93	2511	28.031	75.02	2103	408
72 Hr	28.055	44.75	2511	28.031	75.02	2103	408

4.2 Thermal Control

The Demonstration Module was instrumented with (11) thermocoupler in order to evaluate the thermal control design. The unit was operated at 28 volts input and 28 volts 75 amperes output at room ambient and free convection cooling. These temperatures were monitored during the 72 hour continuous operation test to identify any long range change or component aging. The unit operated satisfactorily during the test.

Table 4- IX presents the data of the temperature rise. The test data illustrates that all component temperature are within component temperature applications.

The hottest temperature rise (94°F) was the internal ambient air temperature near the output filter capacitor A5C3 and A5C4. A review of the component in the area showed that the air temperature rise was due to power loss in the output shunt resistor A2R1. The shunt is mounted on a bakelite base which does not allow heat transfer by conduction into the rear panel A-2. Losses were also noted in the input/output EMI filter hardware.

The front panel temperature rise was 39°F for an absolute value of 117°F which is above 110°F goal. A coat of paint on the back surface of A-1 should increase the thermal resistance of A-1 and reduce the amount of heat flow from the internal air to the front panel.

TABLE 4-IX TEMPERATURE RISE OF DEMONSTRATION MODULE TEST POINTS

Test Points	Temperature rise above ambient °F
Air above Power Magnetic A3T1	85
Rectifier Case A3CR2	92
Heat sink in center of A3Q4-Q5	78
Capacitor case A3C1	79
Air above Capacitor A5 C3, C4	94
Air above Capacitor A5 C1, C2	85
Printed circuit board for A6 (Center)	76
A3 heat sink temperature	70
A4 heat sink temperature	71
A1 front panel (below current and voltages adjustment) R3, R4	39
A2 read panel temperature under A2L1	62

Test Conditions:

free convection cooling

Input 28VDC

Output 28VDC 75 amperes

Internal losses 407 watts

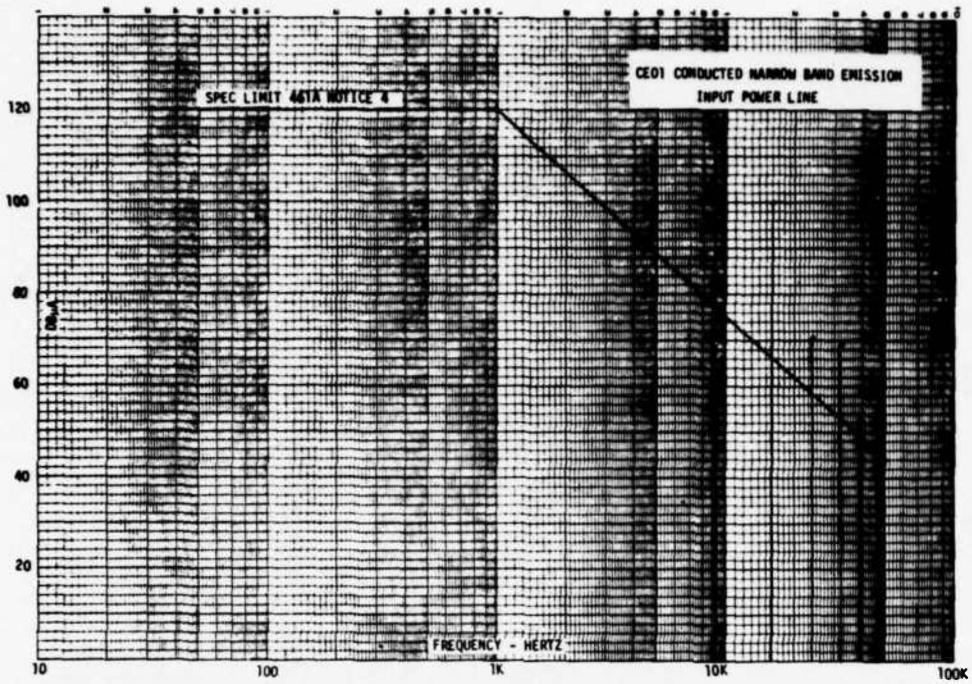
4.3 Electromagnetic Interference Tests

Electromagnetic Interference Tests were performed on the Demonstration Model per MIL-STD-461A. Both conducted and radiated emission tests were performed. The unit was operated from a lead calcium battery power source and at 28V 75A output.

Conducted narrowband and broadband emission tests were performed on the input power line, output power line and remote output sense line.

Figure 4-6 presents the narrowband data on the input power line. The high peak at 64kHz was due to the resonance of the second stage input filter capacitors and the cabling. Addition of the second stage inductor and damping resistance reduces this current reflection into the power source. Figure 4-7 presents the narrowband data on the output power line. Figure 4-8 presents the narrowband data on the remote output sense line. Additional filtering of the remote sense line should reduce the out of tolerance condition in the 70kHz to 300kHz frequency range. Figure 4-9 through 4-11 presents the broadband emission data from the input power line, output power line and remote sense line, respectively. Figure 4-12 and 4-13 presents the narrowband and broadband radiated emission from the demonstration model.

MIL-STD-461A, Notice 4 specification limits are shown on each curve to identify out of tolerance conditions.



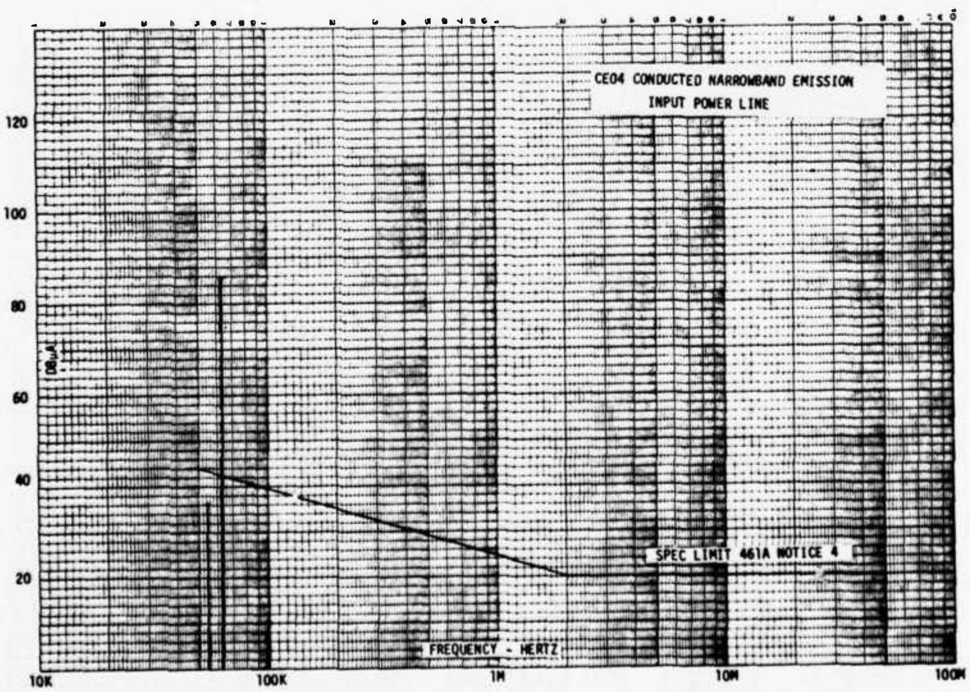
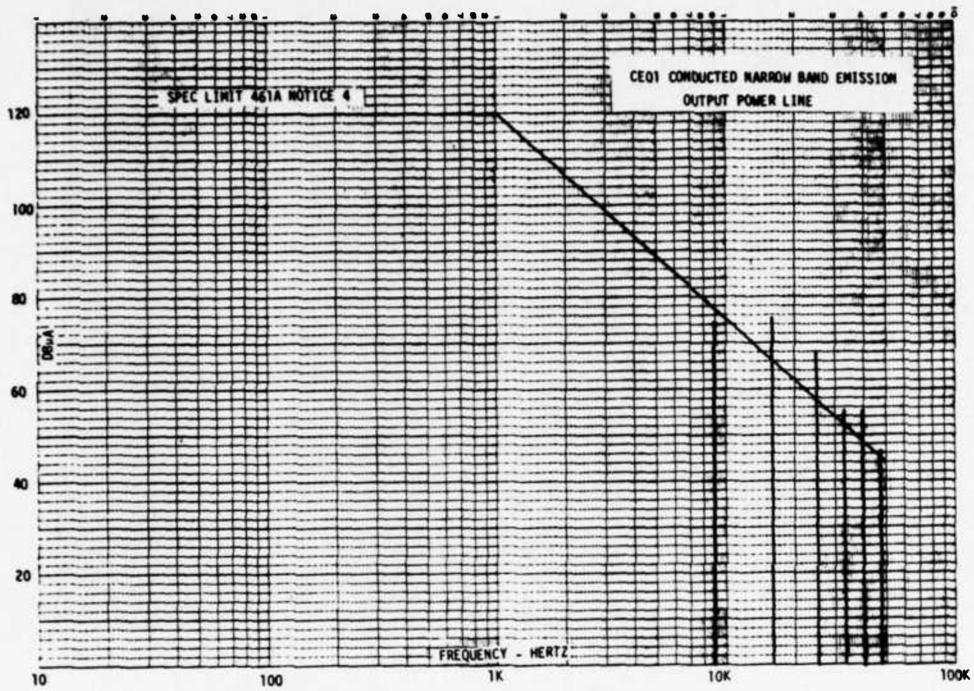


FIGURE 4-6 NARROW BAND EMISSION - INPUT POWER LINE



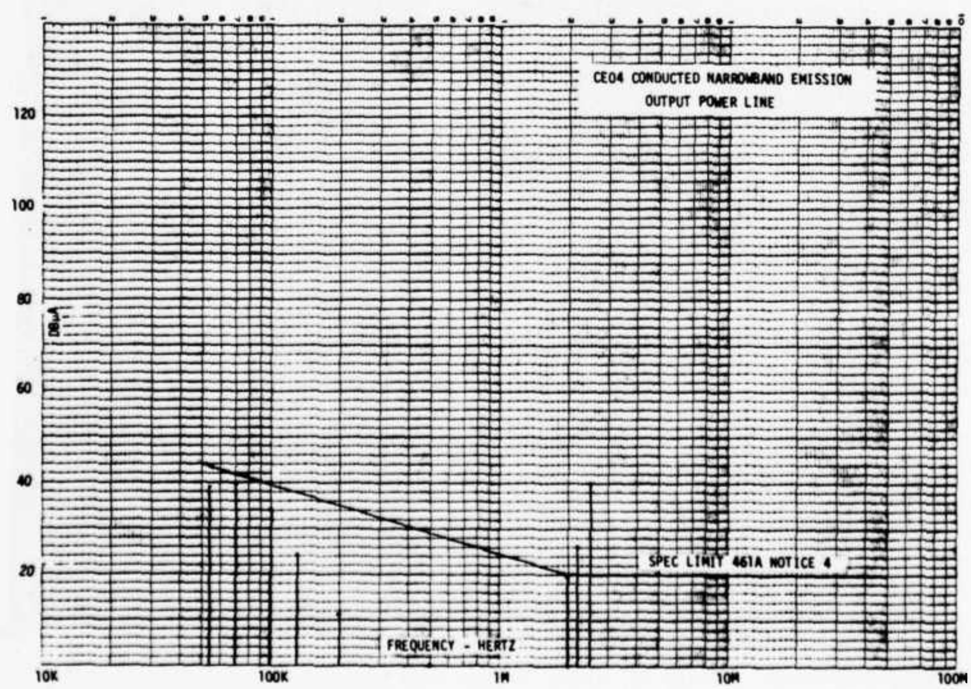
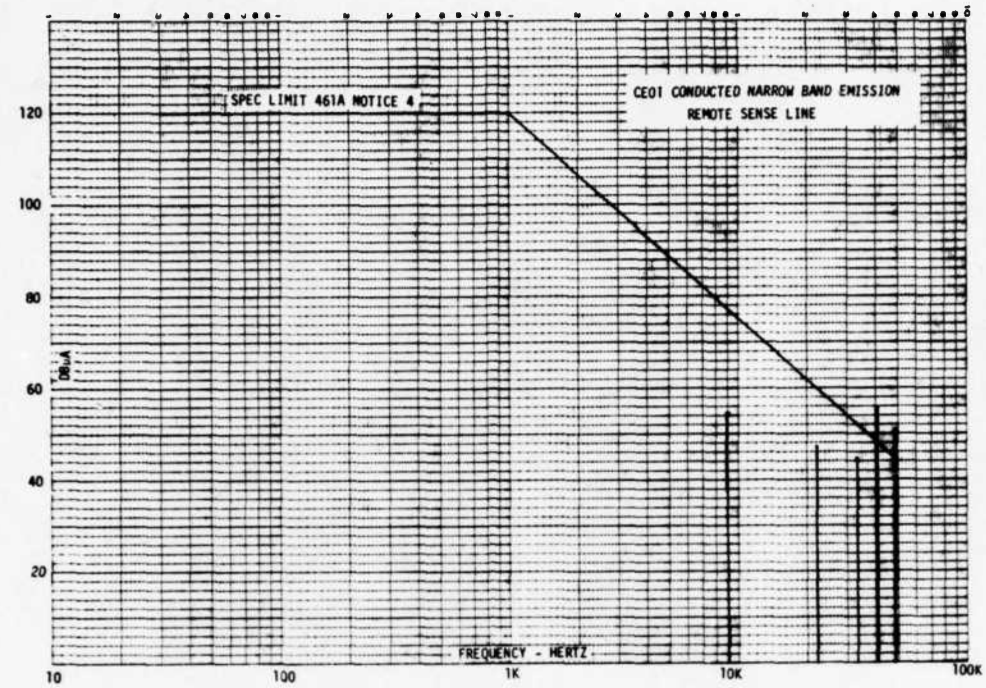


FIGURE 4-7 NARROW BAND EMISSION - OUTPUT POWER LINE



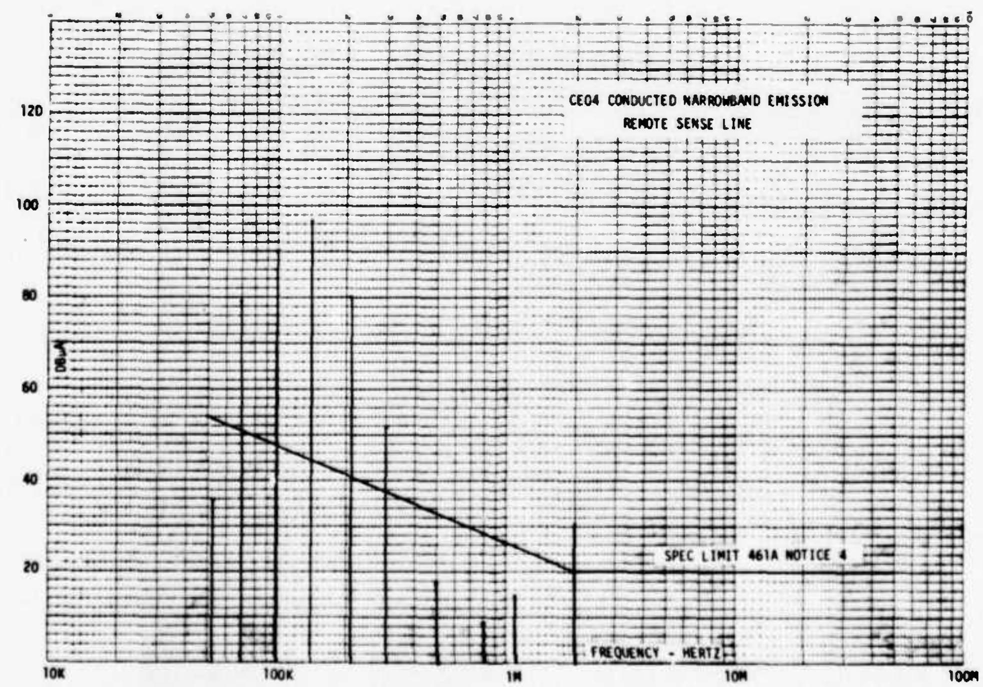


FIGURE 4-8 NARROW BAND EMISSION REMOTE SENSE LINE

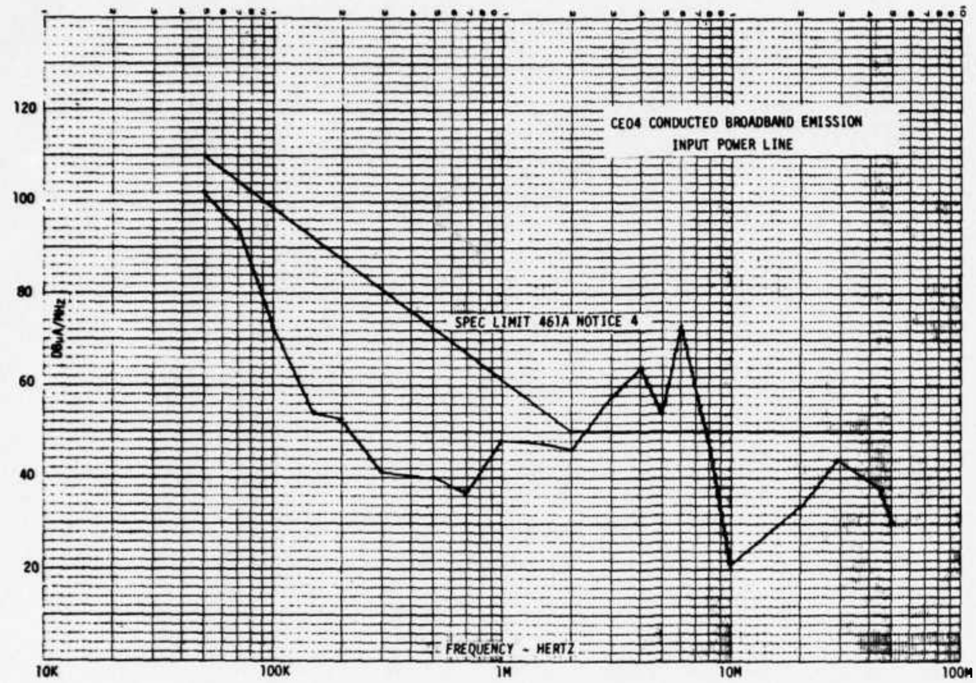


FIGURE 4-9 BROAD BAND EMISSION - INPUT POWER LINE

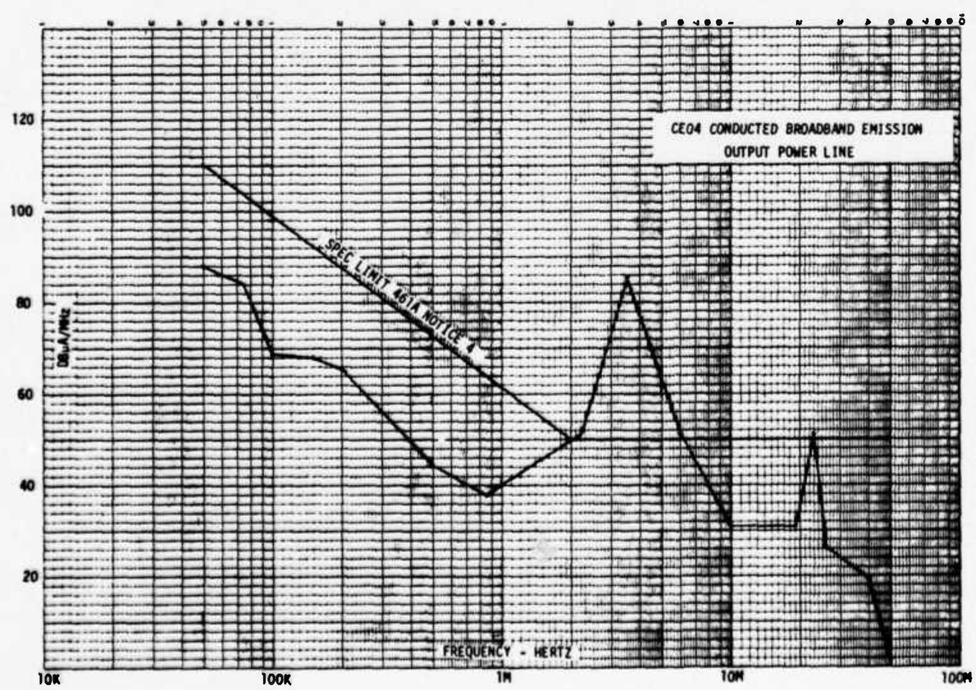


FIGURE 4-10 BROAD BAND EMISSION - OUTPUT POWER LINE

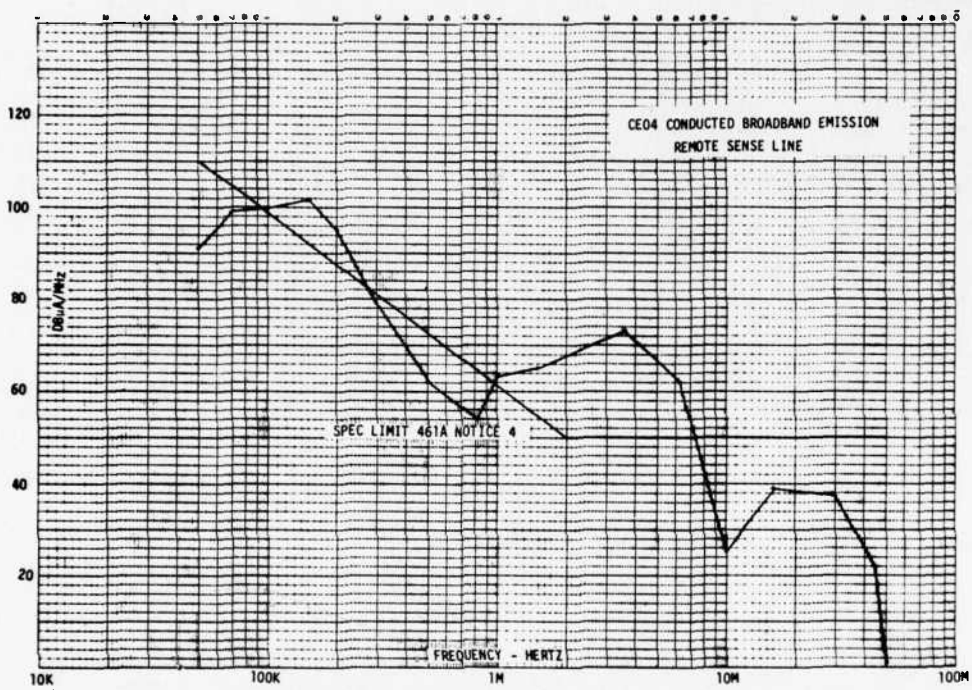
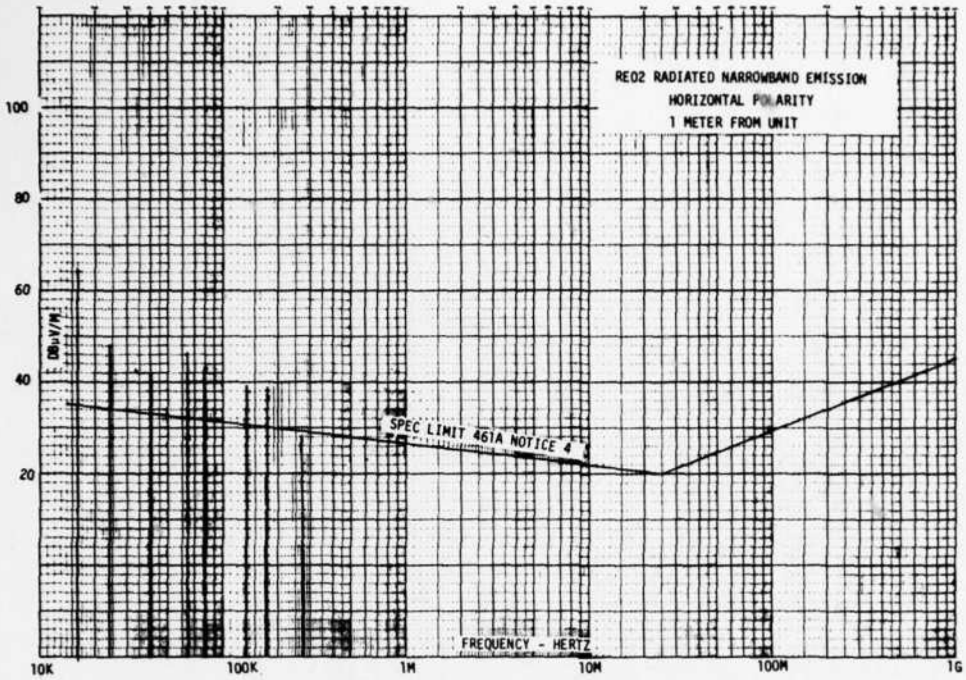
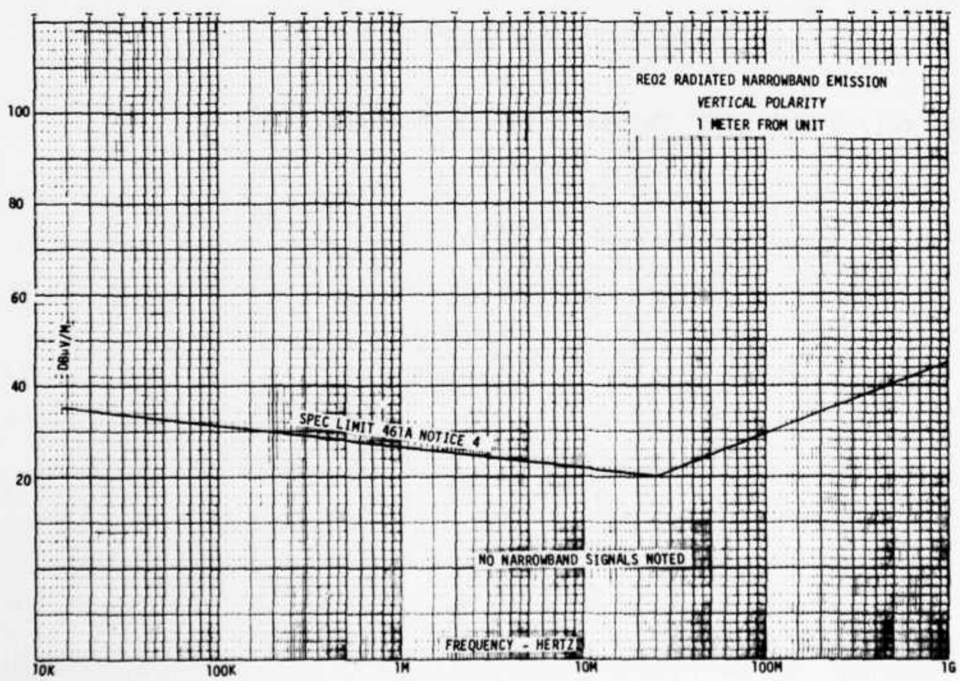


FIGURE 4-11 BROAD BAND EMISSION - REMOTE SENSE LINE

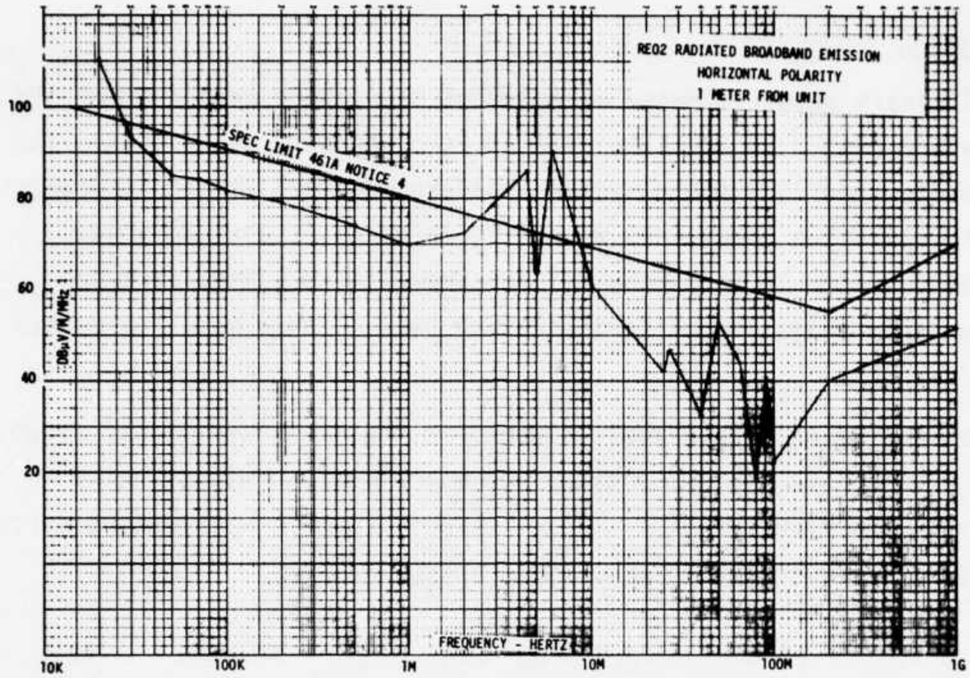


a) HORIZONTAL POLARITY

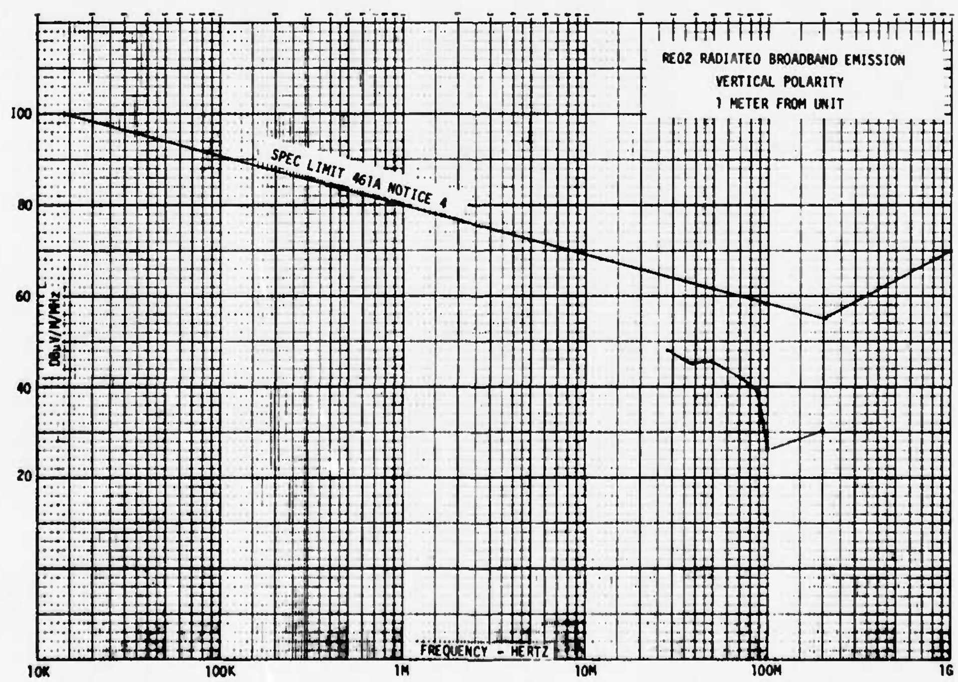


b) VERTICAL POLARITY

FIGURE 4-12 RADIATED NARROW BAND EMISSION



a) HORIZONTAL POLARITY



b) VERTICAL POLARITY

FIGURE 4-13 RADIATED BROAD BAND EMISSION

4.4 Acoustic Noise Tests

Preliminary acoustic noise measurement tests were performed on the Demonstration Unit. Figure 4-14 illustrates the test setup used. The General Radio type 1933 sound system analyzer was used in the "A" Filter mode. The operating conditions were off, 28 volts 75 amp, 28 volts 50 amp and 28 volts 25 amp outputs. Measurements were made from the front and side panels on the demonstration unit. Table 4- X presents the test results.

Noise levels increased above ambient in the 8 KHz and 16 KHz range. The side panels which contains the power magnetics had higher noise reading than the front panel. The noise level varies with output current with maximum level occurring at maximum output current.

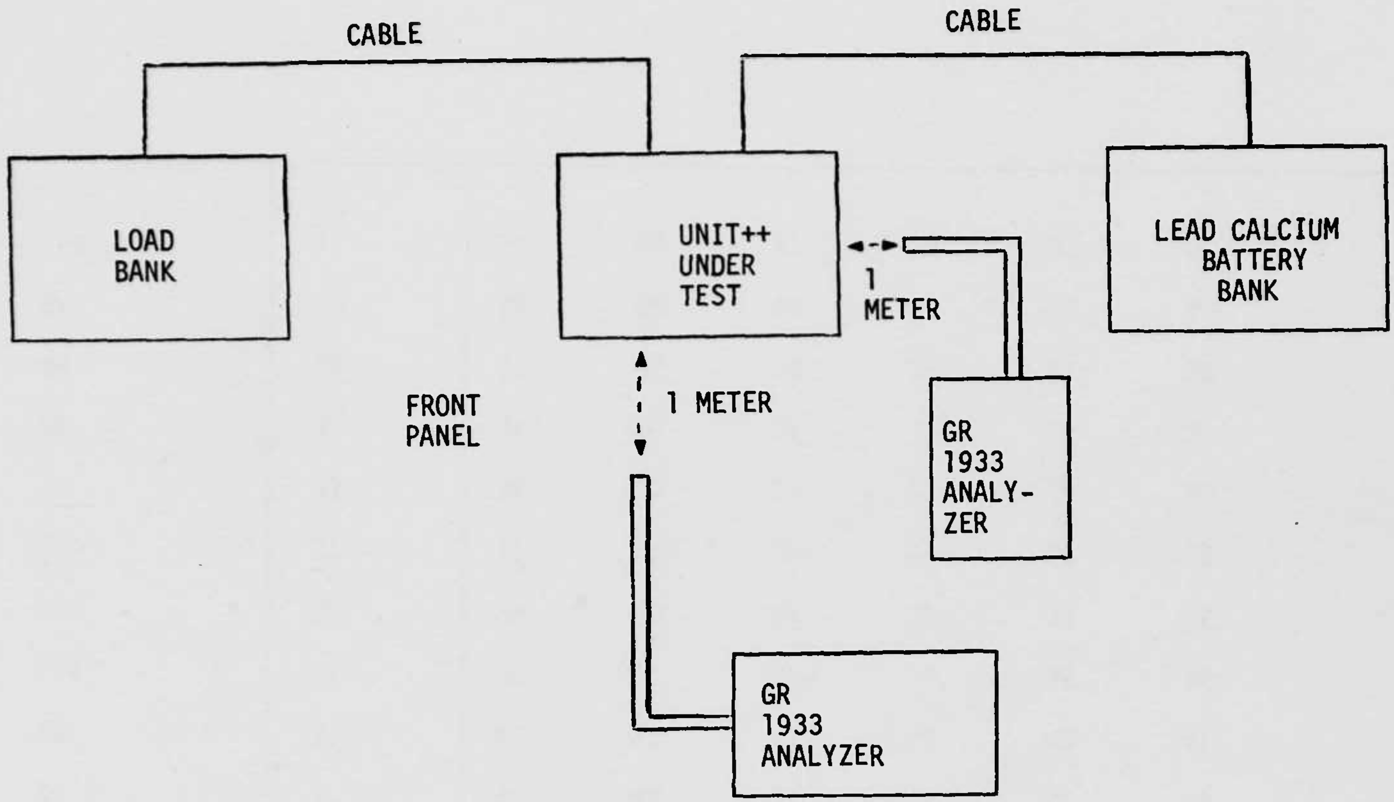


FIGURE 4-14 ACOUSTIC NOISE MEASUREMENT TEST SETUP.

TABLE 4-X ACOUSTIC NOISE MEASUREMENTS OF DC-DC CONVERTER REGULATOR

OCTAVE BAND CENTER FREQUENCY HZ	GENERAL RADIO	SOUND PRESSURE LEVEL DB 1933 ANALYZER 1 FT FRONT UNIT					
	UNIT OFF	75 AMP OUTPUT		50 AMP OUTPUT		25 AMP OUTPUT	
	FRONT	FRONT	SIDE	FRONT	SIDE	FRONT	SIDE
31.5	47	47	44	52	54	52	54
63	43	42	42	44	42	42	41
125	34	35	37	37	36	36	36
200	34	34	36	34	36	34	36
500	37	37	34	36	33	36	33
1K	37	36	32	37	32	36	32
2K	34	34	30	34	31	33	31
4K	29	31	34	32	29	31	29
8K	23	46	54	49	58	40	40
16K	15	54	64	41	54	33	51

5. CONCLUSIONS AND RECOMMENDATIONS

The 2.4kW DC-DC Converter/Regulator described in this report demonstrates a significant advance in power processing technology.

The following is a summary of the milestones accomplished:

1. Development of the transistorized series inductor parallel inverter power stage which protects the power transistor and reduces its peak voltage and power stresses.
2. Phase displaced operation of four separate power modules from one output voltage regulator with excellent regulation and transient response and reduced input/output filtering requirements.
3. Mechanical packaging that facilitates maintainability.
4. Thermal control concept that ensures adequate component operating temperature.

The electrical, mechanical and thermal characteristics demonstrate the basic capability of the 2.4kW DC-DC Converter/Regulator. It fulfills the requirement for the standardized power module for the U. S. Army Communication, Data Handling, Surveilance and Weapons Systems.

Continued component development is required for the power transistor to improve its switching characteristics and thereby reduce losses and improve overall efficiency.

Only minor modifications are required for the EMI filter in order to meet MIL-STD-461A, Notice 4, and for the mounting of the components on the A2 module to reduce the demonstration model internal air temperature when operating in a free convection cooling mode only.

6. REFERENCES

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(2) Baker, D. E. "Aerospace Technology Development of Three Types of Solid State Remote Power Controllers for 120Vdc with Current Ratings of Five and Thirty Amperes, One Type having Current Limiting," NASA CR-134772, Contract NAS3-17771, NASA Lewis Research Center

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(4) Biess, J. J. & Schoenfeld, A.D. "Effect of Requirement Specification on Implementation of a Power Processor," 24th Annual Proceedings Power Sources Symposium, May 19-21 1970

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(10) Schegel, E. S., et. al. "Development of a 1000V, 200A, Low Loss Fast Switching, Gate Assisted Turn-off Thyristor," NASA CR 134951, Contract NAS3-16801, NASA Lewis Research Center

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(13) Schwarz, F. C. & Klassens, J. B. "A Controllable Secondary Multikilowatt DC Current Source with Constant Maximum Power Factor in its Three Phase Supply Line," 1975 Power Electronics Specialist Conference

(14) Yu, Yuan, et. al. "The Application of Standardized Control and Interface Circuits to Three DC to DC Power Converters," IEEE Power Processing & Electronics Specialist Conference 1973

(15) Yu, Y. & J. J. Biess "Some Design Aspects Concerning Input Filters for DC-DC Converters," Power Conversion Specialist Conference 1971

APPENDIX A - PARTS LIST

The following parts list contains the components used on each subassembly.

A1 through A6. The reference designators agree with the schematics presented in Section 3-2 Electrical Design.

CONFIGURATION				PARTS LIST					
QTY REQD	QTY REQD	QTY REQD	QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT	NOMENCLATURE OR DESCRIPTION	SPECIFICATION OR MANUFACTURER	CKT REF	ITEM NO.
			1	AM1516-150		150A SINGLE POLE BKR.	HEINEMANN	CB1	
			1	ZXAM1516-100		100A Z POLE BKR.	"	CB2	
			1	101-5030-971		LIGHT, INDICATOR - RED	DIALITE	LT-1	
			1	330		LAMP, INCANDESCENT - 14V	CHICAGO MINIATURE		
			1	5226-8941		100mV FULL SCALE	WESTON MODEL 2521	M1	
			2	NCH-25-25Ω		25Ω 25W NON-IND. RES.	DALE	R1, 2	
			1	RA20LASB252A		2.5K W/W POT	BOURNS	R3	
			1	RA20LASB201A		200Ω W/W POT	BOURNS	R4	
			1	MS25308-262		4 POLE ON-MOM-ON SWITCH	MIL-S-8834	S1	

TRW SYSTEMS GROUP
ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

SIZE	CODE IDENT NO.		REV
A	11982	A1 FRONT PANEL	
		SHEET	

SYSTEMS 2444 REV. 2-67

CONFIGURATION				PARTS LIST					
QTY REQD	QTY REQD	QTY REQD	QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT	NOMENCLATURE OR DESCRIPTION	SPECIFICATION OR MANUFACTURER	CKT REF	ITEM NO.
			1	1N5816		20A 150V DIODE	UNITRODE	CR1	
			1	T1489-B		9µh IND. 140A	TRW	L1	
			1	9992-0041239		0-100mV SHUNT	WESTON	R1	
			2	L1306		9µh IND 70A	TRW	L2, 3	
			2	RE77G1R00		1Ω 100W RESISTOR	DALE	R2, 3	

TRW SYSTEMS GROUP
ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

SIZE	CODE IDENT NO.		REV
A	11982	A2 REAR PANEL	
		SHEET	

SYSTEMS 2444 REV. 2-67

CONFIGURATION				PARTS LIST					
QTY REQD	QTY REQD	QTY REQD	QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT	NOMENCLATURE OR DESCRIPTION	SPECIFICATION OR MANUFACTURER	CKT REF	ITEM NO.
			4	74F01AB106		10μF 100V POLY	GE	C1-4	
			1	MS3102A-24-125		CONN. 2 x NO. "0"	AMPHENAL	J1	

TRW SYSTEMS GROUP
ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

SIZE	CODE IDENT NO.		REV
A	11982	A2A1 INPUT EMI FILTER	
		SHEET	

SYSTEMS 2444 REV. 2-67

CONFIGURATION				PARTS LIST					
QTY REQD	QTY REQD	QTY REQD	QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT	NOMENCLATURE OR DESCRIPTION	SPECIFICATION OR MANUFACTURER	CKT REF	ITEM NO.
			9	74F01AB106		10μF 100V POLY	GE	C1-9	
			2	650B1C474J		.47μF 200V POLY	GE	C10,11	
			1	MS3102A-32-5P		CONN. 2 #4 3 #16 PINS	AMPHENAL	J1	

TRW SYSTEMS GROUP
ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

SIZE	CODE IDENT NO.		REV
A	11982	A2A2 OUTPUT EMI FILTER	
		SHEET	

SYSTEMS 2444 REV. 2-67

CONFIGURATION				PARTS LIST					
QTY REQD	QTY REQD	QTY REQD A3	QTY REQD A4	PART OR IDENTIFYING NO.	CODE IDENT	NOMENCLATURE OR DESCRIPTION	SPECIFICATION OR MANUFACTURER	CKT REF	ITEM NO.
		8	8	CK06BX473K		.047μF 200V CER	AROUOX	C1-C4, C6-C9	
		1	1	X85D106KXL973		10μF 200V POLY	COMPONENTS RESEARCH	C5	
		1	1	LP8A1B226K		22μF 100V POLY	DEARBORN	C10	
		2	2	SCSF2R		100A DIODE	SEMTECH	CR1, 3	
		2	2	SCSPF2L		100A DUAL DIODE	SEMTECH	CR2, 4	
		1	1	1N3340B		100V 50W ZENER	MOTOROLA	VR1,	
		1	1	M24308/2-2		CONNECTOR 15 SOCKET		J1	
		1	1	M24308/4-2		CONNECTOR 15 PIN		J1	
		8	8	2N6033		60A 130V TRANSISTOR	RCA	Q1-Q8	
				T1471A		CURRENT SENSE TRANSFORMER			
		2	2	T1527A		OUTPUT TRANSFORMER	TRW	T1, 2	
				T1562A		FLYBACK IND.			

TRW SYSTEMS GROUP
ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

SIZE	CODE IDENT NO.		REV
A	11982	A3 & A4 POWER STAGE	
		SHEET	

SYSTEMS 2444 REV. 2-67

CONFIGURATION				PARTS LIST					
QTY REQD A3A1	QTY REQD A3A2	QTY REQD A4A1	QTY REQD A4A2	PART OR IDENTIFYING NO.	CODE IDENT	NOMENCLATURE OR DESCRIPTION	SPECIFICATION OR MANUFACTURER	CKT REF	ITEM NO.
1	1	1	1	M39003/01-2526		10μF 20V TANT CASE "B"	MIL-C-39003	C1	
1	1	1	1	74F01BA105		1μF 200V POLY	GE	C2	
4	4	4	4	1N5417		3A 200V DIODE	SEMTECH	CR1-4	
2	2	2	2	2N2222A		SIGNAL NPN TRANSISTOR		Q1,2	
2	2	2	2	2N4225		5A 50V TRANSISTOR		Q3,4	
2	2	2	2	T1463E		CURRENT DRIVE TRANSFORMER	TRW	T1,2	
4	4	4	4	RWR81S2000FR		200Ω 1W W/W ±1%	MIL-R-39007	R1,2,7,8	
2	2	2	2	RWR81S2500FR		250Ω 1W W/W ±1%	MIL-R-39007	R3,4	
2	2	2	2	RCR07G163JS		16K 1/4W ±5%	MIL-R-39008	R5,6	

TRW SYSTEMS GROUP
ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

SIZE	CODE IDENT NO.		REV
A	11982	A3A1 & A3A2 - A4A1 & A4A2 DRIVE AMPLIFIER	
		SHEET	

SYSTEMS 2444 REV. 2-67

CONFIGURATION				PARTS LIST					
QTY REQD	QTY REQD	QTY REQD	QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT	NOMENCLATURE OR DESCRIPTION	SPECIFICATION OR MANUFACTURER	CKT REF	ITEM NO.
			2	92F282ALA		12000μF 75VDC/100VDC SURGE	GE	C1,2	
			2	92F233ALA		5600μF 40VDC/55VDC SURGE	GE	C3,4	
			1	T1471A		CURRENT SENSE TRANSFORMER	TRW	T1	

TRW
SYSTEMS GROUP
ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

SIZE	CODE IDENT NO.		REV
A	11982	A5 INPUT & OUTPUT FILTER	-
		SHEET	

SYSTEMS 2444 REV. 2-67

CONFIGURATION				PARTS LIST					
QTY REQD	QTY REQD	QTY REQD	QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT	NOMENCLATURE OR DESCRIPTION	SPECIFICATION OR MANUFACTURER	CKT REF	ITEM NO.
			1	74F01AB106		10μF 100V POLY	GE	C1	1
			1	650B1C474J		.47μF 200V POLY	GE	C2	2
			2	69F335G8		170μF 15V TANT	GE	C3,11	3
			20	CKR06BX104		.1μF 100V CER	MIL-C-39014	(C4,7,16-18,27-30 39-49)	4
			1	69F435		540μF 15V TANT	GE	C6	5
			7	CKR06BX103		.01μ 200V CER	MIL-C-39014	C8,12,15 31-34	6
			1	M39003/01-2734		4.7μF 10V TANT	S_RAGUE	C9	7
			2	CM30E222J		.0022μF MICA	MIL-C-5	C10,14	8
			1	39003/01-2517		150μF 15V TANT	MIL-C-39003	C13	9
			4	CM30E562J		.0056μF MICA	MIL-C-5	C35-38	10
			1	CKR05BX102		.001μ 200V CER	MIL-C-39014	C5	11
			8	CKR05BX100		10 PF 200V CER	"	C19-26	12
			1	CKR05270		27PF 200V CER	"	C50	13
			1	CKR05680		68PF 200V CER	"	C51	14
			1	1N756A		8.2V 400mV ZENER	MOT.	VR1	15
			3	1N4573A		6.4V 1mA REF. ZENER	MOT.	VR2-4	16
			1	1N3595		100mA 100V DIODE	MOT.	CR6	17

TRW
SYSTEMS GROUP
ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

SIZE	CODE IDENT NO.		REV
A	11982	A6 CONTROL ELECTRONICS	
		SHEET	

SYSTEMS 2444 REV. 2-57

CONFIGURATION				PARTS LIST					
QTY REQD	QTY REQD	QTY REQD	QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT	NOMENCLATURE OR DESCRIPTION	SPECIFICATION OR MANUFACTURER	CKT REF	ITEM NO.
			3	1N5417		3A 200V DIODE	SEMTECH	CR1-3	18
			11	1N3600		100mA 100V DIODE	MOT.	CR4,5, CR7-15	19
			1	2N5415		PNP 1A 300V TRANSISTOR	RCA	Q2	20
			1	2N3440		NPN 1A 300V TRANSISTOR	RCA	Q3	21
			4	2N2907A		PNP LOW LEVEL TRANSISTOR	MOT.	Q4-7	22
			1	2N5804		5A - 300V POWER TRANSFORMER	RCA	Q1	23
			4	SBR05F		BRIDGE RECTIFIER	SEMTECH	Z1-4	24
			3	LM111D		IC COMPARATOR	NATIONAL	U1,5,6	25
			1	µA7805KM		IC 5V REGULATOR	FAIRCHILD	U2	26
			2	HA2-2520-2		IC OPER. AMP	HARRIS	U3,4	27
			1	SE555V		IC TIMER	INTERSIL	U7	28
			1	5082-4351		IC OP-COMP-ISOL	H.P.	U8	29
			1	CD4018AE		IC RING COUNTER	RCA	U9	30
			2	DM5404N		IC HEX INVERTER	NATIONAL	U10,11	31
			4	SN54221J		IC DUAL 1-SHOT	T.I.	U12-15	32

TRW SYSTEMS GROUP
ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

SIZE	CODE IDENT NO.		REV
A	11982	A6 CONTROL ELECTRONICS	
		SHEET	

SYSTEMS 2444 REV. 2-67

CONFIGURATION				PARTS LIST					
QTY REQD	QTY REQD	QTY REQD	QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT	NOMENCLATURE OR DESCRIPTION	SPECIFICATION OR MANUFACTURER	CKT REF	ITEM NO.
			1	DM5408N		IC QUAD "AND"	NATIONAL	U16	33
			4	SE556A		IC DUAL TIMER	SIGNETICS	U17-20	34
			1	LM139D		IC QUAD COMP	NATIONAL	U21	35
			4	SN55452BJG		IC DRIVER PERIPHERAL DUAL	T.I.	U22-25	36
			2	RCR20G103JS		RESISTOR 10K 1/2W ±5%	MIL-R-39008	R1,4	
			1	RWR80S2001FR		" 2K 2W W/W ±1%	MIL-R-39007	R2	
			1	RCR07G121JS		" 120Ω 1/4W W/W ±1%	MIL-R-39008	R3	
			3	RCR05G513JS		" 51K 1/8W W/W ±1%	MIL-R-39008	R5,30,31	
			1	RNC55H3571FR		" 3.57K 1/10W ±1%	MIL-R-55182	R6	
			1	RCR05G102JS		" 1.0K 1/8W ±5%	MIL-R-39008	R7	
			1	RNC55H6341FR		" 6.34K 1/10W ±1%	MIL-R-55182	R8	
			4	RNC55H1002FR		" 10K 1/10W ±1%	MIL-R-55182	R9-11,13	
			1	C259558-102		" 100Ω TRIM POT	BOURNS	R12	
			1	RCR05G915JS		" 9.1MΩ 1/8W ±5%	MIL-R-39008	R14	
			1	C25955R-105		" 1.0K TRIM POT	BOURNS	R15	

TRW SYSTEMS GROUP
ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

SIZE	CODE IDENT NO.		REV
A	11982	A6 CONTROL ELECTRONICS	
		SHEET	

SYSTEMS 2444 REV. 2-67

CONFIGURATION				PARTS LIST					
QTY REQD	QTY REQD	QTY REQD	QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT	NOMENCLATURE OR DESCRIPTION	SPECIFICATION OR MANUFACTURER	CKT REF	ITEM NO.
			1	RNC55H4641FR		RESISTOR 4.64K 1/10W ±1%	MIL-R-55182	R16	
			1	RNC55H2002FR		" 20.0K 1/10W ±1%	"	R17	
			2	RCR07G392JS		" 3.9K 1/4W ±5%	MIL-R-39008	R18,32	
			1	RCR05G104JS		" 100K 1/8W ±5%	"	R19	
			1	RCR05G821JS		" 820Ω 1/8W ±5%	"	R20	
			1	RCR05G201JS		" 200 1/4W ±5%	"	R21	
			3	C259558-107		" 5.0K TRIM POT	BOURNS	R22,24,67	
			1	RNC55H5111FR		" 5.11K 1/10W ±1%	MIL-R-55182	R23	
			1	RNC55H1502FR		" 15.0K 1/10W ±1%	"	R25	
79			3	RNC55H3011FR		" 3.01K 1/10W ±1%	"	R26,28,72	
			2	RCR05G302JS		" 3K 1/8W ±5%	MIL-R-39008	R27,40	
			1	RNC55H3651FR		" 3.65K 1/10W ±1%	MIL-R-55182	R29	
			1	RCR05G623JS		" 62K 1/8W ±5%	MIL-R-39008	R33	
			2	RCR05G204JS		" 200K 1/8W ±5%	"	R34,41	
			1	RNC55H2872FR		" 28.7K 1/10W ±1%	MIL-R-55182	R35	
			1	RNC55J2402FR		" 24.9K 1/10W ±1%	"	R36	
			1	RNC55H1961FR		" 1.96K 1/10W ±1%	"	R38	

TRW
SYSTEMS GROUP
ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

SIZE	CODE IDENT NO.		REV
A	11982	A6 CONTROL ELECTRONICS	
		SHEET	

SYSTEMS 2444 REV. 2-67

CONFIGURATION				PARTS LIST					
QTY REQD	QTY REQD	QTY REQD	QTY REQD	PART OR IDENTIFYING NO.	CODE IDENT	NOMENCLATURE OR DESCRIPTION	SPECIFICATION OR MANUFACTURER	CKT REF	ITEM NO.
			1	RCR07G101JS		RESISTOR 100Ω 1/4W ±5%	MIL-R-39008	R39	
			3	RCR07G512JS		" 5.1K 1/4W ±5%	"	R42,44,78	
			1	RCR07G561JS		" 560Ω 1/4W ±5%	"	R43	
			12	RCR05G103JS		" 10K 1/8W ±5%	"	R45-52 R68-71	
			4	RNC55H3832FR		" 38.3K 1/10W ±1%	MIL-R-55182	R53-56	
			4	RCR05G682JS		" 6.8K 1/8W ±5%	MIL-R-39008	R57-60	
			5	C259558-109		" 20K TRIM POT	BOURNS	R37,61-64	
			3	RNC55H1001FR		" 1.0K 1/10W ±1%	MIL-R-55182	R65,66,73	
			4	RWR81S61R9FR		" 61.9Ω 1W W/W ±1%	MIL-R-39007	R74-77	
			2	M24308/2-3		CONNECTOR 25 SOCKET		J1,2	
			2	M24308/4-3		CONNECTOR 25 PIN		J1,2	

TRW SYSTEMS GROUP
ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

SIZE	CODE IDENT NO.		REV
A	11982	A6 CONTROL ELECTRONICS	
		SHEET	

SYSTEMS 2444 REV. 2-67

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